IEEE/ACM
2026 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
ICCAD
45th Edition

CALL FOR PAPERS

DEADLINES

April 7, 2026
Abstract Submissions

April 14, 2026
Paper Submissions

April 14, 2026
Proposal Submissions (Workshops, Tutorials, Special Sessions, Panels)

June 8, 2026
Notifications for Workshops, Tutorials, Special Sessions, Panels

June 10, 2026
Reviews Shared with Authors for Rebuttals

June 17, 2026
Author Rebuttals Submissions

July 11, 2026
Notifications for Regular Papers

August 24, 2026
Camera-Ready Paper Submission Deadline

August 24, 2026
Author Registration Deadline

Jointly sponsored by IEEE and ACM, ICCAD 2026 explores the full spectrum of electronic design automation, extending from device-level physics to system-level architecture. Building on a long-standing tradition of technical excellence, ICCAD delivers a cutting-edge program that spans fundamental areas such as logic synthesis, verification, physical design, simulation, reliability, and manufacturing alongside critical system-level topics including embedded systems, IoT, and cyber-physical systems. The conference addresses emerging challenges in 3D ICs, chiplets, and advanced packaging, as well as hardware security, low-power computing, and reconfigurable architectures. Furthermore, the scope encompasses the intersection of AI and hardware, ranging from AI for CAD and CAD for AI accelerators to physical AI for embodied intelligence, while investigating future paradigms such as quantum, neuromorphic, and post-CMOS computing.

COVERED TOPICS

Original technical submissions on, but not limited to, the following topics are invited:

» **System-Level CAD**
- **System Modeling:** HW/SW co-design, simulation, & heterogeneous SoCs.
- **AI & Accelerators:** Neural network hardware, AI algorithms, & CAD for AI.
- **Embedded Systems & Edge Computing:** Cyber-physical systems, FPGAs, & CGRAs.

» **Synthesis, Verification, Physical Design Analysis, Simulation, & Modeling**
- **Logic Synthesis:** Technology mapping & optimization.
- **Physical Design:** Floorplanning, placement, routing, & CTS.
- **Verification & Test:** Formal verification, emulation, ATPG, & post-silicon debug.
- **Analysis:** Timing, power, and signal integrity optimization.

» **Emerging Technologies and Paradigms**
- **Nanoscale & Post-CMOS:** Emerging devices, nanophotonics, & CAD for mixed-domain & field-coupled technologies.
- **Advanced Computing Paradigms:** Non-von Neumann architectures, quantum computing, DNA computing, neuromorphic hardware, swarm intelligence & green computing.

Please note we are migrating to **hotcrp.com** for paper/proposal submissions. More details on the covered topics and the submission process will be shared on the ICCAD website.

CALL FOR PROPOSALS

In addition to technical session presentations, the IEEE/ACM ICCAD will also include:

- Workshops
- Tutorials
- Special sessions
- Panels

ORGANIZING CHAIRS

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More information is available at iccad.com.

IEEE/ACM ICCAD

Original technical submissions on, but not limited to, the following topics are invited:

1) System-level CAD

1.1 System Design

- System-level specification, modeling, simulation, etc.
- System-level issues for 3D integration
- System-level design case studies and applications
- HW/SW co-design, co-simulation, co-optimization, and co-exploration; emulation and rapid prototyping
- Micro-architectural transformation
- Multi-/many-core processor and heterogeneous SoC
- Memory and storage architecture and system synthesis
- System communication architecture, Network-on-Chip design
- Modeling, simulation, high-level synthesis, power/performance analysis, programming of heterogeneous computing platforms
- Application driven system design for big data
- Analysis and optimization of data centers or cloud systems
- AI for system design

1.2 Embedded, CPS, IoT Systems and Software

- HW/SW co-design for embedded systems
- Compute, memory, storage, interconnect for embedded systems
- Domain-specific accelerators
- Energy/power management and energy harvesting
- Real-time software and systems
- Middleware, virtual machines, and runtime support
- Dependable, safe, secure, trustworthy embedded systems
- Embedded software: compilation, optimization, testing
- CAD for IoT, edge, and fog computing
- Modeling, analysis, verification of CPS systems
- Green computing (smart grid, energy, solar panels, etc.)

1.3 AI Algorithms and Applications

- New AI algorithms and applications
- New AI-driven design methodology
- AI algorithms and applications for embedded, CPS, IoT systems
- AI algorithms and applications on edge or in the cloud
- AI surrogate modeling for devices and circuits
- Agentic AI and autonomous design assistants
- Large language models (LLMs) for design & verification (GenAI for EDA)
- Data-Centric EDA: Datasets, cleaning, and benchmarking
- Explainable and trustworthy AI (XAI) for CAD

1.4 CAD for AI

- CAD for AI accelerator design
- HW/SW co-design for AI algorithms and accelerators
- Neural architecture search for AI algorithms
- CAD for edge AI or online learning
- CAD for AI systems design in the cloud
- CAD for AI hardware on emerging technologies
- AI+HW Co-design

1.5 Hardware Systems and Architectures for Artificial Intelligence

- Hardware and architecture for AI
- Architecture designs for Edge AI and TinyML
- System-level design for (deep) neural computing
- Neural network acceleration including GPUs, NPUs, and ASICs

1.6 Reconfigurable Computing

- Novel reconfigurable architectures (FPGA, CGRA, etc.)
- Neural network acceleration on reconfigurable accelerators
- High-level synthesis on reconfigurable architectures
- Compilers for reconfigurable architectures
- Reconfigurable fabric security
- HW/SW prototyping and emulation on FPGAs
- Post-synthesis optimization for FPGAs
- FPGA-based prototyping for analog, mixed-signal, RF systems
- AI for Reconfigurable Computing

1.7 Algorithms and Computing for Security

- New physical attack vectors or methods
- Supply chain security and anti-counterfeiting
- Privacy-preserving computation
- Homomorphic encryption and computation
- Zero knowledge proof
- AI for security
- Security and privacy for AI algorithms and applications

1.8 Architecture and Systems for Security

- Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- Nano electronic security
- Hardware-based security (CAD for PUF's, RNG, AES etc.)
- Split Manufacturing for security
- Design and CAD for security
- Trusted execution environments
- Cloud Computing data security
- Sensor network security
- Hardware Security for AI Models (Model Protection)

1.9 Low Power and Approximate Computing

- Power and thermal estimation, analysis, optimization, and management for hardware and software systems
- Energy and thermal-aware architectures, application mapping, and scheduling
- Dynamic power and thermal management algorithms
- System-level design for dark silicon and heterogeneity
- Hardware techniques for approximate/stochastic computing
- AI for low power and approximate computing

1.10 3D IC's, Chiplets, and Advanced Packaging

- Advanced packaging & heterogeneous integration
- Stress, warpage, and reliability analysis for stacked dies
- Vertical power delivery networks: backside power delivery, TSV planning, and IR-drop mitigation
- Chiplet interface & interconnect standards
- Thermal physics and advanced cooling solutions

1.11 PHYSICAL AI & EMBODIED INTELLIGENCE

- Co-design of neural control, sensor morphology, mechanical dynamics under size, weight, power, cost constraints
- CAD for software-defined vehicles, drones, humanoids, and industrial cobots
- Design automation for wearables, soft robotics, bio-hybrid systems, and human-robot collaboration
- Differentiable physics, reality gap modeling, and digital twins for industrial automation
- Sim-to-real adaptation and robust control under environmental variability
- Hardware architectures for sensorimotor loops, vision-language-action models, and edge foundation models
- Near-sensor and in-sensor computing for milliwatt-scale robotics and sensor fusion
- Functional safety compliance, verification, and runtime monitoring of learning-enabled systems

IEEE/ACM ICCAD

2) SYNTHESIS, VERIFICATION, PHYSICAL DESIGN, ANALYSIS, SIMULATION, AND MODELING

2.1 High-Level and Logic

- New high-level/logic synthesis techniques
- Technology-independent optimization and technology mapping
- Functional and logic ECO (engineering change order)
- Resource scheduling, allocation, and synthesis
- Interaction between high-level/logic synthesis and physical design
- Acceleration algorithms for high-level/logic synthesis
- AI for high-level/logic synthesis

2.2 Testing, Validation, Simulation, and Verification

- High-level/logic modeling, validation, simulation
- Formal, semi-formal, and assertion-based verification
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon validation and debug
- Digital fault modeling and simulation analysis and optimization
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test
- AI for testing, validation, simulation, and verification

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- Cell library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning,. floor planning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning
- AI for physical design

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level routing and optimization
- Chip-package-board co-design
- Layout and routing issues for optical interconnects
- Post-layout/-silicon optimization
- AI for clock network synthesis, routing, and post layout optimization and verification

2.5 Design for Manufacturability and Design for Synthesis and Optimization Reliability

- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical verification and design rule checking
- Analysis and optimization for device-level reliability issues
- Analysis optimization for interconnect reliability issues
- Reliability issues related to soft errors
- Design for resilience and robustness
- AI for smart manufacturing and process control
- Advanced electromigration analysis
- Device aging and degradation modeling
- Robust power delivery network design
- Signoff for mission-critical applications

2.6 Timing, Power, and Signal Integrity

- Deterministic and statistical static timing analysis, optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization
- AI for timing, power, and signal integrity

2.7 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- Analog, mixed-signal, and RF noise modeling, simulation, test
- Electromagnetic simulation and optimization
- Device, interconnect, and circuit extraction and simulation
- Behavior modeling of devices and interconnect
- Package modeling and analysis
- AI for analog/mixed-signal/RF and multi-domain modeling

3) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS

3.1 Bio-inspired and Neuromorphic Computing

- Hardware for neuromorphic computing
- Event or spike-based hardware systems
- CAD for microfluidics
- CAD for biological computing systems
- CAD for synthetic biology
- CAD for bio-electronic devices, bio-sensors, MEMS

3.2 New System and Computing Paradigms

- Non-von Neumann architectures
- Quantum computing, algorithms, and applications
- Quantum and classical computing integration
- DNA computing
- Swarm intelligence
- Green computing
- Hyperdimensional computing
- New technologies for AI (e.g. optical or quantum neural networks, large-scale chiplet-based systems).

3.3 Nanoscale and Post-CMOS Systems

- New device structures and process technologies
- New memory technologies (e.g. flash, PCM, STT-RAM, memristor)
- Nanotechnologies, nanowires, nanotubes, graphene, etc.
- CAD for mixed-domain (semiconductor, nano-electronics, MEMS, and electro-optical) devices and systems
- CAD for nano-photonics and optical devices/ communication
- CAD for field-coupled nanotechnologies
- Device, interconnect and circuit extraction and simulation
- Behavior modeling of nanodevices and emerging interconnects

SUBMISSION DETAILS

Please note that we are using a new submission framework this year as follows:

- Regular Papers: Submit via **iccad2026.hotcrp.com**
- Invited Papers, Tutorials, and Special Session Proposals: Submit via **iccad2026-proposals.hotcrp.com**
- Workshop Proposals: Submit via **https://forms.gle/fFcnWYVwiRkEawmAA**

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar) with the camera-ready version if the paper has been accepted. For protecting the authors' identities in the double-blind review process, please do not include a direct link to the non-anonymized software but indicate the open-source contribution on a textural basis only. Authors wishing to share GitHub repositories may want to look into using anonymous.4open.science which is an open-source tool that helps you to quickly double-blind your repository. Authors are asked to submit their works in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via iccad2026.hotcrp.com. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for declaring COIs, ensuring that their paper submission meets all guidelines, and that the PDF is readable.

Special Session organizers and speakers may submit papers via **iccad2026-proposals.hotcrp.com**. These will be considered invited papers. Please use the following guidelines when submitting the camera-ready versions of these papers:

1. Each co-author may contribute only one special session paper in the entire ICCAD'26 program.
2. Include a paper abstract, author list, and designated speaker for each presentation in your session
3. Titles and author lists are final and cannot be altered, unless per feedback from the ICCAD 2026 Special Sessions and Tutorials Technical Program Committee
4. Speaker assignments are fixed and cannot be modified, unless per feedback from the ICCAD 2026 Special Sessions and Tutorials Technical Program Committee
5. No additional special session papers can be submitted other than those mentioned in the proposal
6. Please add the key word "Invited" before the camera-ready version title of the paper
7. Follow the same copyright release procedure as the regularly submitted papers

Panel Session organizers and speakers may submit a single paper on the panel topic, with all speakers (and organizers, if appropriate) listed as co-authors.

Tutorial Session organizers and speakers cannot submit papers. Only Tutorial Session proposals are required.

Please refer to additional details for preparing proposals below.

REGULAR PAPER SUBMISSIONS

- The abstract submission deadline is April 7, 2026 at 23:59 AOE. *NO abstract submissions will be possible after this deadline.*
- The paper submission deadline is April 14, 2026 at 23:59 AOE.
- We always have several authors contact the IEEE/ACM ICCAD office asking for a deadline extension. *Due to the limited review cycle, NO extensions will be granted for ANY reason.*
- Papers must be submitted as PDFs. Ensure the text is selectable (not a scanned image) and that all fonts inside your graphics are properly embedded.
- Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. One page of references is allowed, which does not count towards this 8-page limitation.
- IEEE/ACM ICCAD follows a double-blind review policy. Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the authors' own published works or affiliations should be made in the third person.
- Submissions of workshop papers without archived proceedings (or where the authors chose not to have their paper appear in the archived proceedings) or pre-prints, e.g., published on arXiv are allowed. Note, however, that the authors are expected to follow all reasonable efforts to ensure that the submission is compliant with the double-blind review process.
- Submissions not adhering to these rules or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected.
- For any related questions please email the Program Chair, Ismail Bustany, at ismail.bustany@amd.com
- Submissions must be made through **iccad2026.hotcrp.com**

PUBLICATION FEE GUIDELINES

Important Change: Different from previous years, ICCAD is adopting the ACM Open Access publishing guidelines; as such, an Article Processing Charge (APC) will be charged to all published papers.

This APC is a per-paper fee determined by the status of the designated corresponding author: $250 for ACM/SIG members and $350 for non-members. However, if the corresponding author's institution participates in the ACM Open Access program, this fee is automatically waived. For the list of participating institutions and full policy information, please visit https://authors.acm.org/open-access.

Authors from low-income countries generally receive a full waiver (100% discount), while authors from lower-middle-income countries receive further discounted rates (50% discount). The list of such countries and the corresponding discount is here: **https://www.acm.org/publications/policies/waiver-countries**. The remaining authors (not participating in ACM Open Access program and not qualifying for a geographic waiver) may apply for a financial hardship waiver, supported by SIGDA and the SIG Governing Board. If approved, the authors will receive a 100% discount on the APC.

Eligibility Criteria for SIGDA-Supported Financial Hardship Waivers: SIGDA-supported Financial Hardship Waivers are subject to the following eligibility criteria:

1. SIGDA Membership

» The corresponding author must be a current SIGDA member (please join through Membership - SIGDA if not a member) at the time of the request.

2. ACM Open Access Coverage Check

» The paper is not already covered by an ACM Open Access institutional or national agreement.

» If any author is affiliated with an ACM Open Access participating institution, SIGDA support does not apply.

3. Financial Hardship Justification

» Authors must provide a short-written statement describing the financial hardship as part of the ACM eRights waiver request.

» Typical (non-exclusive) examples include:

- Students without institutional publication or travel support.
- Early-career researchers without active grants.
- Authors from under-resourced institutions or low-income regions.

4. Industry Papers (Exclusion)

» Papers authored by industry researchers are not eligible for SIGDA financial support.

» In such cases, it is expected that the employing company provides publication support for the APC.

5. Scope of Support

» The waiver applies only to the ACM/SIG member APC ($250).

» SIGDA does not provide support beyond this amount.

Determination of APC:

1. The corresponding author must complete the publication steps in the ACM eRights system.
2. ACM eRights determines whether the paper is:
   a. Covered by an ACM Open institutional or national agreement (no APC required), or
   b. Subject to an APC, with automatic discounts applied where eligible (e.g., ACM/SIG membership, country-based discounts).
3. If an APC remains and represents a barrier, the corresponding author may submit a Financial Hardship Waiver (FHW) request directly within ACM eRights.
4. FHW requests are reviewed and approved or declined through the established ACM and SIG workflows before publication can proceed.
5. If the request is declined, the authors can still decide to pay for the APC. Otherwise, the paper will not be published.
6. The corresponding author cannot be changed after the paper has been accepted.

PAPER TEMPLATES

Authors of regular and invited papers must format their papers according to the IEEE/ACM paper templates available at **www.iccad.com/authors**.

CAMERA-READY VERSIONS

Final camera-ready versions must be identical to the submitted papers with the following exceptions: Inclusion of author names/affiliation, correction of identified errors, addressing reviewer demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules.

REBUTTAL PROCESS

Instructions for the regular paper rebuttal process will be published on **www.iccad.com/authors.**

PAPER TEMPLATES

Paper templates are available at the IEEE/ACM ICCAD website and authors are recommended to format their papers based on the IEEE ACM template.

NOTIFICATION OF ACCEPTANCE

Regular Paper Submission Authors will be notified of acceptance on July 11, 2026. Final paper guidelines will be sent at that time.

Tutorial, Special Session, and Panel proposal authors will be notified of acceptance on June 8, 2026. Final paper guidelines (where applicable) will be sent at that time.

CONFERENCE PROCEEDINGS

The deadline for final camera-ready papers is August 24, 2026. Accepted regular papers or invited papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at $150.00 per page up to the eight-page plus one page of references. ACM will hold the copyright for ICCAD 2026 proceedings. Authors of accepted papers must sign an ACM copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or invited paper must be registered to the conference by August 24, 2026. Failure to register will result in your paper being removed from the conference proceedings. IEEE/ACM reserves the right to exclude a paper from distribution after the conference (e.g., removal from the official proceedings) if the paper is not presented at the conference.

IEEE/ACM WILLIAM J. MCCALLA-ICCAD BEST PAPER AWARD

Two papers from this year's IEEE/ACM ICCAD conference will receive this prestigious award. The winners will be chosen from nominated papers by the area specific selection committees after a thorough and competitive process and announced at the conference opening session.

IEEE/ACM ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2016 and 2017 editions of IEEE/ACM ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community as reflected in citations, on the vendor community via its use in an industrial setting, or on new research venues as initiated by the paper during the past decade. Nominations from the community are welcome and can be sent to Tsung-Yi Ho, Program Vice Chair, at **tyho@cuhk.edu.hk**.

WORKSHOP, TUTORIALS, AND SPECIAL SESSION PROPOSALS

WORKSHOP PROPOSALS

IEEE/ACM ICCAD provides a vibrant and supportive environment for small to medium-sized affiliated workshops. Typical workshops are one-day or half-day events on the Thursday of IEEE/ACM ICCAD. Please contact the ICCAD Workshop Chair Hai Helen Li at hai.li@duke.edu for any questions.

Workshop proposals must be submitted via **forms.gle/fFcnWYVwiRkEawmAA** by April 14, 2026.

TUTORIAL PROPOSALS

All IEEE/ACM ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants/speakers with biographical data. Proposals should focus on the state-of-the art in a specific area of broad interest amongst IEEE/ACM ICCAD attendees. All tutorial proposals should be submitted through the IEEE/ACM ICCAD website and questions can be addressed to Ron Duncan, Tutorial and Special Sessions Chair, at **ron.duncan@synopsys.com**. Please read the proposal guidelines at IEEE/ACM ICCAD website.

SPECIAL SESSION AND PANEL SESSION PROPOSALS

Special Sessions or Panel Sessions typically run 1.5-2 hours. Special/Panel Ssession proposals should focus on in-depth treatment of a topic of timely interest to the IEEE/ACM ICCAD audience. Such proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants/speakers with biographical data. All such proposals should be submitted through the IEEE/ACM ICCAD website and questions can be addressed to Ron Duncan, Tutorial and Special Sessions Chair, at ron.duncan@synopsys.com. Please read the proposal guidelines at IEEE/ACM ICCAD website. Submitted papers must follow the same ACM proceeding guidelines for regular conference paper submissions. You must include the designation (Invited Paper) in the paper title.

Tutorial and Special Session proposals must be submitted via **iccad2026-proposals.hotcrp.com** by April 14, 2026.

ICCAD WORKFORCE DEVELOPMENT ACTIVITIES

ICCAD offers a rich set of student-oriented activities, including the Student Research Competition (SRC), CADathlon, EDA Job Fair, the CAD Contest at ICCAD, and the Student Scholar Program, to provide students with diverse platforms for learning, competition, networking, and professional development in the field of Electronic Design Automation (EDA).

- The Student Research Competition (SRC) allows undergraduate and graduate students to present their research, exchange ideas with peers and experts, and gain recognition through an internationally respected ACM-sponsored competition.
- The CADathlon is an intensive, all-day team programming contest that challenges students with practical and cutting-edge EDA problems while emphasizing algorithmic thinking, implementation skills, and teamwork.
- The Job Fair connects students and early-career researchers with leading industry and academic employers, offering opportunities for internships, postdoctoral positions, and full-time roles through structured introductions and open networking.
- The CAD Contest at ICCAD is a multi-month global research competition where teams address real-world EDA challenges proposed by industry, fostering long-term collaboration between academia and industry and producing impactful research outcomes.
- The Student Scholar Program provides need-based financial support to enable students to attend ICCAD and actively participate in presentations, competitions, and networking activities. For more details about these student activities and participation opportunities, please visit the official ICCAD website www.iccad.com.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

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