DVCON U.S. 2027

March 1-4, 2027 | Santa Clara, CA, USA

2027 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

CALL FOR EXTENDED ABSTRACTS

ORGANIZERS

General Chair
Xiaolin Chen
Synopsys

Program Committee Chair
Dave Rich
Arteris

Program Committee Vice-Chair
Peter George
Independent

IMPORTANT DATES & DEADLINES

July 15, 2026
Submission Site Opens

September 7, 2026
Abstract Submission Deadline

October 1, 2026
Abstract Preliminary Accept/ Reject Notification

November 1, 2026
Draft Paper Submission Deadline

December 1, 2026
Paper Preliminary Accept/Reject Notification

December 23, 2026
Final Paper Submission/Author Registration Deadline

January 14, 2027
Paper Final Accept/Reject Notification

February 7, 2027
Final Poster/Slides/Video Deadline

All deadlines are 11:59 PM Pacific Time on the date listed.

Feel free to contact us for questions on the submission process at lleblanc@conferencecatalysts.com or visit DVCon.org.

The Design & Verification Conference is looking for submissions for the in-person 2027 Conference and Exhibition. This conference focuses on the practical aspects of design and verification of electronic systems and integrated circuits. This could be applications of languages, tools, methodologies, and/or standards. This could be your chance to help the industry we are all a part of. For those familiar with DVCon, the submission timeline has changed for this year. Please see below for more details.

DVCon honors the **Stuart Sutherland** Best Paper Award. The awards will be selected by the attendees at DVCon, based on the quality of both the paper and their presentation. Awards will be offered for both slide and poster presentation formats. **So please submit your abstract and join DVCon U.S. 2027!**

Please submit your extended abstract outlining your proposed presentation by **Monday, September 7**. Full instructions and details for the extended abstract submission process can be found on **dvcon.org.**

Because of the delayed submission deadline for DVCon U.S. 2027, extensions will not be provided at any point during the submission process. If the guidelines/deadlines are not followed, DVCon will remove your submission.

EXTENDED ABSTRACT SUBMISSION GUIDELINES

The extended abstract should provide enough details so that the Technical Program Committee (TPC) can evaluate the potential quality of your completed paper and the interest of the DVCon attendees in your presentation.

An extended abstract is expected to include the following details:

- Proposed paper title
- An introduction that specifies the context and motivation of the submission.
- A clear description of the specific contributions of your work.
- A summary that highlights results.
- References, if appropriate.
- Must use the provided template format (found on the DVCon website).
- Must be a minimum of 600 words - maximum of 1,200 words, approximately 2 pages.
- Submission should be double-blind, please remove the author information.

Preliminary accepted authors agree to do the following:

- Submit a draft paper by **November 1**
- Review and incorporate feedback from Technical Program Committee (TPC)
- Submit a final paper and copyright form by **December 23**. This Final paper will be reviewed by the Technical Program Committee (TPC) to determine Final Accept/Reject status
- Submission indicates your agreement to present it orally onsite either as a slide or a poster presentation, should it be accepted

Final accepted authors agree to do the following:

- Review and incorporate feedback from Technical Program Committee (TPC)
- Submit a final presentation/poster by **February 7**
- Submit a recorded presentation (in case we need to change back to a virtual conference) by **February 7**

By submitting this proposal, you are committing to personally attend the conference and deliver the material if it is accepted. Should you be unable to attend in person, it is required that you give a minimum of 4 weeks' notice before the conference begins to enable the technical committee time to arrange a replacement. Failure to provide adequate notice will result in your inability to propose a paper for the next two years.

CALL FOR EXTENDED ABSTRACTS Cont.

This call for abstracts solicits for papers and corresponding presentations that are highly technical and reflect real-life experiences and emerging trends in various domains. Submissions are encouraged in (but not restricted to) the following areas:

Coverage Strategies and Optimization

» Coverage closure, analysis techniques, machine learning-guided coverage, and test efficiency

Formal and Assertion-based Verification

» Scalable formal methods, assertion-driven flows, formal applications, and methodology

Clocking, Timing, and CDC/RDC Verification

» Clock/reset-domain crossing techniques, timing constraints, asynchronous logic, and domain verification

Modern Testbench Architecture and Language Integration

» UVM design patterns, reuse strategies, SoC testbenches, Python/C++ co-simulation, DPI, and PSS

Functional Safety and Compliance

» ISO 26262, DO-254, fault injection, safety coverage, and verification metrics

Processor and Custom Architecture Verification

» RISC-V cores, custom instruction set architecture extensions, compliance testing, and microarchitecture verification

Security Verification and Trust in Hardware

» Side-channel analysis, data leakage prevention, secure boot, and hardware trust modeling

Regression Management, CI/CD in Verification Workflows

» Automation pipelines, debug triage, result clustering, cloud flows, and DevOps/GitOps for verification

Requirements Traceability and Spec Linking

» Spec-to-test traceability, audit readiness, natural language processing tools, and requirements-driven verification

Mixed-Signal and AMS Verification

» Analog/mixed-signal integration, RNMs, co-simulation with digital, and behavioral modeling

Low Power Design and Verification

» UPF methodologies, dynamic power-aware simulation, power state modeling, and assertions

FPGA Prototyping for Verification Acceleration

» Pre-silicon validation with FPGA, hybrid flows, debug methodologies, and integration challenges

Emulation and System-Level Validation

» Hardware/software co-verification, pre-silicon debug, SoC bring-up, software development, virtual prototyping

CONFERENCE SCHEDULE

Monday, March 1

» Sponsored Tutorials
» Sponsored Workshops

Tuesday, March 2

» Technical sessions
» Keynote Speaker
» Exhibits

Wednesday, March 3

» Technical Sessions
» Panel Discussions
» Exhibits

Thursday, March 4

» Sponsored Tutorials
» Sponsored Workshops