CALL FOR PANELS

DVCON US 2027

March 1-4, 2027 • Santa Clara, CA

2027 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is the usage of specialized design and verification languages such as SystemVerilog, Verilog, VHDL, PSS, SystemC and e, as well as general purpose languages such as C, C++, Python, PERL and Tcl. Tools and methodologies include the use of artificial intelligence, machine learning, open-source software, hardware and architecture, testbench automation, hardware-assisted verification, hardware/software co-verification, formal verification, functional safety and security, transaction-level system design, high level synthesis, low power design techniques, 3D chip designs, IP-based SoC design methods, reference flows and Mixed Signal design and verification.

Conference attendees are primarily designers and verification engineers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development, and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using these languages and tools.

PANEL PROPOSAL

Deadline: November 1, 2026

Proposals: Submit online at DVCon.org.

DVCon is planning to host one highly focused panel discussion. DVCon is looking for a panel that is lively, controversial, and provokes discussion on a specific topic of interest to the community. The panel session should not consist of a paper presentation, but should have plenty of discussion engaging the audience. The panel is scheduled for 1 hour on Wednesday, March 3, 2027.

Please make sure that the moderator and panelists are available on Wednesday, March 3, 2027. DVCon will attempt to work with the original organizer in refining the panel, but if this is not successful, another organizer may be appointed. If multiple panel suggestions are submitted with similar topics, the committee may choose to accept one over the others, to merge the proposed panels, or to reject all of them.

TOPIC SUGGESTIONS

We invite you to contribute your knowledge and experience within the hardware design and verification, advanced tools, and new methodologies areas, and to participate in the valuable exchange of ideas. Panels should combine experiences in a given area with forward-looking statements regarding technology and industry trends, and challenges likely to be encountered as the state of the art continues to progress.

- Experiences using design and/or verification IP for System- on-Chip development
- Experiences applying machine-learning techniques
- Security validation and verification
- Experiences adopting functional-safety related standards such as ISO26262, DO-254 etc.
- Dealing with the technical and logistical challenges of multi-site projects
- Developing, adopting and proliferating new standards
- Experiences deploying a verification methodology library, especially deployment of UVM
- Designing and/or verifying complex ASICs and FPGAs using multiple HDLs and/or HVLs in a design cycle
- Open-source tools and applications in design and verification

PROPOSAL SUBMISSION

Proposals should be 2-3 pages in length and should contain:

- The topic, if possible formulated as a provocative question
- The issues to be discussed, including a short listing of pro and con arguments
- Short biographies of the moderator and prospective panelists
- Any special requirements

PANEL SCHEDULE

November 1, 2026: Proposal Deadline
December 4, 2026: Accept/Reject notification
January 8, 2027: Final panel title, abstract and panelists names due for website

CONFERENCE SCHEDULE

Monday, March 1: Sponsored Tutorials & Workshops
Tuesday, March 2: Technical Sessions, Keynote Speaker, Poster Session, Exhibits
Wednesday, March 3: Technical Sessions, Panel Discussion, Exhibits
Thursday, March 4: Sponsored Tutorials & Workshops

For more information concerning the conference, please contact conference management:
Conference Catalysts | Laura LeBlanc | lleblanc@conferencecatalysts.com

Conference Sponsor:

accellera SYSTEMS INITIATIVE

Panel Chair
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Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**