CALL FOR SHORT WORKSHOPS

DVCON US 2026

March 2-5, 2026 • Santa Clara, CA

DVCon is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus is on specialized design and verification languages such as SystemVerilog, Verilog, VHDL, PSS, SystemC, and e, as well as general-purpose languages like C, C++, Python, Perl, and Tcl. Tools and methodologies include artificial intelligence, machine learning, open-source software, hardware and architecture, testbench automation, hardware-assisted verification, hardware/software co-verification, formal verification, functional safety and security, transaction-level system design, high-level synthesis, low-power design techniques, 3D chip designs, IP-based SoC design methods, reference flows, and mixed-signal design and verification.

DVCon offers short workshops to increase sponsor and exhibitor participation, especially for smaller companies. DVCon is seeking short workshop topics that are current, highly relevant, and educational. Sponsors reach a captive audience during the 90-minute sessions and can follow up with attendees during breaks, at the exhibits, and after the event.

DVCon is a highly targeted venue for engineers addressing major design and verification challenges. Submit proposals by **Sunday, September 7**. For suggested topics and the timeline, see page 2.

DVCON Sponsored Short Workshop: $5,500

Sponsorship Includes:

- One 90-minute workshop presentation on either Monday or Thursday (workshop timeslot will be selected by the committee)
- Your company logo on DVCon U.S. website, promotions, program, proceedings, and more
- The right to distribute or display promotional materials, such as banners, flyers, and gift items, during your workshop
- One complimentary one-day conference registration for the day of your workshop

Sponsored workshops will be reviewed and approved by the program committee with respect to technical depth and applicability. In case of multiple organizations presenting a sponsored workshop only the organizing company would get the sponsorship benefits mentioned above.

For more information concerning the conference, please contact the conference management, Laura LeBlanc at lleblanc@conferencecatalysts.com

Detailed guidelines for preparing the presentations will be made available after selections are final.

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2026 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

SHORT WORKSHOP PROPOSAL REQUIREMENTS

Deadline: Sunday, September 7, 2025

DVCon short workshops are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the short workshop.

- Attendee expectations are high regarding currency of topic, depth of engineering content and breadth of real-life examples
- The Workshop Chair will review final presentation materials to ensure high quality educational content
- Include suggested presenters names, affiliations & biographies
- Your proposal should be a short abstract of the workshop, two to five paragraphs, 1,000 words maximum
- Presentation slides need to be supplied in an electronic format in advance of the conference. Presentation slides will be distributed to the attendees in electronic format. Hard copies will not be provided
- Please indicate if this workshop is a "hands-on" session or lecture format
- Any necessary additional hardware that you may require must be provided by the workshop organizers

SUGGESTED TOPICS

DVCon workshops are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the workshop.

- SystemVerilog for Verification and/or Design
- SystemC /C/C++ Design and/or Verification of systems.
- SoC and Software-driven Verification
- Assertion-based Verification. SystemVerilog Assertions, PSL, etc.
- Coverage-driven Verification
- High-level Synthesis
- Low-power Design and Verification techniques
- Secure/Encrypted IP-based SoC design methods
- Debug for design and verification
- Mixed-signal modeling and verification
- Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT)
- Functional Safety
- Security
- Embedded software verification
- Hardware/Software Co-development
- Verification Productivity Methods
- Formal Methodology and Static Analysis
- Emulation
- Post SI Debug
- FPGA Prototyping
- Moving from proprietary solutions to standards-based design and verification
- Portable Stimulus
- Application-specific design verification challenges and techniques
- Machine Learning applications for verification and design
- Open source hardware/software/architecture

SHORT WORKSHOP DEADLINES

September 7, 2025: Proposals due. Submit at **DVCon.org**

October 2, 2025: Accept/Reject notification

November 2, 2025: All Short Workshop content due for Conference Program and website: workshop title, abstract, speaker names, affiliations and biographies

January 7, 2026: Draft Presentation slides due to DVCon Workshop Chair

February 2, 2026: Presentation feedback due to presenters on slides

February 9, 2026: Final slides due for final production for attendee distribution

CONFERENCE SCHEDULE

Monday, March 2:
- Accellera Day Tutorials
- Short Workshops
- Exhibits

Tuesday, March 3:
- Technical Sessions
- Keynote Speaker
- Poster Session
- Exhibits

Wednesday, March 4:
- Technical Sessions
- Panel Discussions
- Exhibits

Thursday, March 5:
- Tutorials
- Short Workshops

Conference Sponsor:

accellera SYSTEMS INITIATIVE

General Chair
Xiaolin Chen, Synopsys

Workshop Chair
Shekar Chetput, Cadence Design Systems

Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**