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GENERAL CHAIR'S WELCOME

SEE YOU AT THE NEW DAC !

DEAR COLLEAGUE:

It is a great pleasure to welcome you to the 48th edition of the Design Automation Conference in San Diego. In the age of web-conferencing DAC is changing its format to provide the maximum opportunity for multi-way interaction at the conference. In addition to the kickoff reception on Sunday, DAC will feature a reception at the end of each day to stimulate intermingling of all DAC participants from the exhibit floor to the technical sessions. In the technical program, all paper presentations are shortened and immediately followed by a poster session where a dialogue can take place between the author and the audience. At the Wednesday reception the Work In Progress (WIP) session will take place. This new initiative will provide a forum for new ideas, not yet fully ready for a publication, to be exchanged with other experts in the field.

DAC features four keynotes this year. On Monday afternoon we will kick-off with an "Up Close and Personal" with Steve Wozniak. On Thursday we will close the keynote series with a look at the future of computing. Dharmendra S. Modha, IBM, will describe a project to build brain-like cognitive computing chips that scale to human cortex.

DAC is dramatically increasing its focus on Embedded Systems and Software (ESS). On Tuesday Lisa Su, Freescale Semiconductor, will discuss the megatrends that drive Embedded Multi-Core Innovation. Her keynote will outline the evolution of embedded multicore processing solutions that are increasingly enabling the device and infrastructure markets. On Wednesday, Gadi Singer, Intel Corp., will comment on ESS impact on the EDA industry. His keynote will highlight opportunities for innovation and the changes necessary to support this brisk evolution and value creation in electronic systems. Wednesday will feature an ESS Executive day, to provide managers with timely information to help them make decisions where business and technology in ESS domain intersect. More than 30% of the technical program, special sessions and panels are focused on Embedded Systems and Software.

DAC will feature a vibrant exhibition showcasing nearly 200 companies, including all of the largest EDA vendors and significant foundries. At the exhibition we will have a special ESS Zone and IP SOC Pavilion.

DAC has changed the tutorial format. Each tutorial participant can now select three two-hour courses from an exciting collection of six tutorials. All tutorials will take place on Monday this year.

DAC's Technical Program Committee (TPC) has worked hard to present an outstanding technical program this year. The TPC selected 156 papers of the 690 submissions (23% acceptance) for presentation in 4 parallel tracks, covering the entire gamut of topics including Embedded Systems & Software, front-end, back-end, and test. A separate Special Session track will present hot topics and emerging technologies. An exciting set of panels will address topics covering a broad range of Embedded Systems & Software, EDA and emerging areas. Finally, the DAC technical program continues to extend the User Track. This program, specifically designed for EDA tool users, features presentations and poster sessions that highlight outstanding solutions to critical design and methodology challenges, and case studies of innovative tool use.

The number of DAC workshops has almost doubled to eleven. A new all-inclusive registration package will give you access to all of them. Topics range from Smart Grid, Cloud computing and Parallel Algorithms to Inter Vehicle Networking.

An impressive constellation of 12 colocated events complements the DAC program: this includes established conferences and symposia such as AHS, CELUG, DFM&Y, HOST, IWBDA, IWLS, NANOARCH, SASP, and SLIP as well as events focusing on PDKs and OpenAccess scripting.

As organizers of the event, we work with DAC's sponsors and hundreds of volunteers to make it worth your time to attend. I am looking forward to see you all at DAC in San Diego, June 5-9!!

LEON STOK
GENERAL CHAIR, 48TH DAC

SPONSORS

ACM

ACM, the Association for Computing Machinery, is the world's largest educational and scientific computing society, uniting computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the computing profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. www.acm.org

ACM/SIGDA

The ACM Special Interest Group on Design Automation has a long history of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Booth and Ph.D. Forum at DAC, and the CADathlon at ICCAD, and also funds various scholarships and awards. Other benefits provided to SIGDA members include the SIGDA's E-Newsletter containing information on upcoming conferences and funding opportunities, SIGDA News highlighting most relevant events in EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. For further information on SIGDA's programs and resources, see http://www.sigda.org.

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

The IEEE is the world's leading professional association for the advancement of technology, with 400,000 members across 160 countries. The IEEE Council on Electronic Design Automation (CEDA) provides a single focal point for all EDA activities across six major IEEE societies (Circuits & Systems, Computer, Electron Devices, Solid State Circuits, Antennas & Propagation, and Microwave Theory & Techniques). The Council sponsors or co-sponsors over a dozen key EDA conferences, including the Design Automation Conference (DAC), and the International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE) and events at Embedded Systems Week (ESWeek). The Council also publishes the IEEE Transactions on CAD, as well as the IEEE Embedded Systems Letters, and sponsors active technical committees like the DATC and CANDE. Since its founding, the Council has expanded its support of emerging areas within EDA such as nanoscale systems, sponsored new initiatives including the Distinguished Speaker Series and is increasing recognition of members of the EDA profession via awards such as the A. Richard Newton Award, Phil Kaufmann Award, and Early Career Award. The Council welcomes new volunteers and local chapters. For more information on CEDA, visit: www.c-eda.org.

EDA CONSORTIUM

The EDA Consortium (EDAC) is the international association of companies that provide tools and services enabling engineers to create the world's electronic products. EDAC addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation, coordinating software anti-piracy efforts, a quarterly Market Statistics Service (MSS) report, and publication of an industry Operating Systems Roadmap. Companies that become EDAC members are eligible for a 10% discount on DAC Exhibit Booth and Suite Space. Contact the EDA Consortium today about sponsorship and membership opportunities. For more information on the EDA Consortium, visit: www.edac.org.

IMPORTANT INFORMATION

EXHIBIT HOURS

LOCATION Halls D - H

HOURS

Monday, June 6	9:00am - 6:00pm
Tuesday, June 7	9:00am - 6:00pm
Wednesday, June 8	9:00am - 6:00pm

REGISTRATION

LOCATION Lobby D

HOURS

Sunday, June 5	7:30am - 6:00pm
Monday, June 6 - Thursday, June 9	7:00am - 6:00pm

INFORMATION DESK

The Information Desk will be located in the Lobby D of the San Diego Convention Center. Dial (619) 525-6203.

FIRST AID ROOM

The First Aid Room is located in Lobby D of the San Diego Convention Center. For assistance, call ext. 5490; for an emergency, call ext. 8080. A nurse will be on duty at all times while meetings and exhibits are open. Dial (714) 765-8950.

Help may be reached 24 hours a day from any house phone within the San Diego Convention Center.

48TH DAC PROCEEDINGS DVD

Additional copies of the 48th DAC Proceedings DVD may be ordered prepaid from:

ACM Order Department
P.O. Box 11414, New York, NY, 10286-1414
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ATRENTA

STAY CONNECTED AT DAC

WIRELESS INTERNET Sponsored by: 48 DESIGN AUTOMATION CONFERENCE

DAC is offering complimentary wireless internet throughout the San Diego Convention Center. Look for SSID: DAC2011.

MOBILE DEVICES

DAC has a special website built for access from handheld mobile devices. From your smartphone, featurephone, or tablet log in to www.dac.com and you will be automatically redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

DAILY UPDATES ON DAC.COM

Check the DAC website daily for a complete listing of each day's schedule, the latest exhibitor announcements, and press coverage.

FOOD COURT Sponsored by: SYNOPSYS®

The food court is located in Hall G on the exhibit floor and includes tables with power connections for laptop plug-in.

DACNET - 2011

DACnet internet stations are available on the 2nd level by room 33 and on the exhibit floor in the food court.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the San Diego Convention Center, Tuesday, June 7 / 7:00 - 8:30pm. To arrange a BOF meeting, please sign up at the Information Desk located in Lobby D. A meeting room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

ACCESS THE CONFERENCE PROGRAM WITH A QR CODE:

WELCOME TO SAN DIEGO!

SAN DIEGO ATTRACTIONS

San Diego has many world famous attractions. From the San Diego Zoo, to Sea World, to the many natural wonders this city has to offer, there is always something fun and exciting to see and do! Within walking distance of the Convention Center is San Diego's Gaslamp Quarter. This National Historic District features many dining options, shopping and premier entertainment.

WEATHER

San Diego has beautiful weather year round and has an average temperature of 71 degrees. There is no typical day in San Diego, due to the topography of the location. You may experience anything from coastal, mountain and desert environments, just in one day! Days in San Diego are sunny and evenings are pleasingly cool, so be sure to bring a light jacket. With an average of 300 sunny days per year, you are sure to have a great day while in San Diego!

VISIT WWW.SANDIEGO.ORG FOR MORE INFORMATION

or call the San Diego Convention and Visitors Bureau at (619) 232-3101.

HOTEL LOCATIONS:

MONDAY KEYNOTE

June 6

Sponsored by: MAGMA®

2:00 - 3:00pm **Room: 20AB**

UP CLOSE AND PERSONAL WITH STEVE WOZNIAK

STEVE WOZNIAK

Fusion-io, San Jose, CA

SUMMARY:

Steve Wozniak will be interviewed live on stage by San Jose Mercury News columnist Mike Cassidy on a wide range of topics, including the 'joy' of engineering and following your passion to convert innovative ideas into reality. Steve will provide a unique insight into the vision that started the largest and most successful technology company in the world.

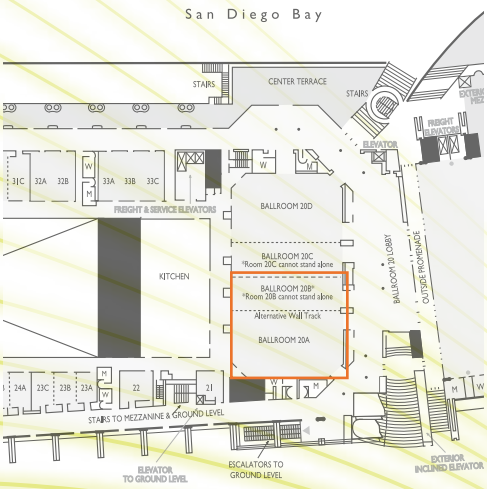
BIO:

A Silicon Valley icon and philanthropist for more than thirty years, **Steve Wozniak** has helped shape the computing industry with his design of Apple's first line of products the Apple I and II and influenced the popular Macintosh. In 1976, Wozniak and Steve Jobs founded Apple Computer, Inc. to market Wozniak's Apple I personal computer. For his achievements at Apple Computer, Inc., Wozniak was awarded the National Medal of Technology, the highest honor bestowed on America's leading innovators.

Since the 1980's, Wozniak has been involved in various business and philanthropic ventures. He has spent a great deal of time and energy focusing on computer usage in schools by stressing hands-on learning and encouraging creativity for students. In 2000, he was inducted into the Inventors Hall of Fame and was awarded the prestigious Heinz Award for Technology, the Economy and Employment. Wozniak also co-founded the Electronic Frontier Foundation, and was the founding sponsor of the Tech Museum, Silicon Valley Ballet and Children's Discovery Museum of San Jose. He currently serves as Chief Scientist for Fusion-io.

TUESDAY KEYNOTE

June 7



8:30 - 10:00am **Room: 20AB**

MEGATRENDS DRIVING EMBEDDED MULTICORE INNOVATION

LISA SU

Freescale Semiconductor, Inc., Austin, TX

SUMMARY:

Internet traffic is dramatically increasing, and the fastest growing segment, mobile network traffic, is expected to double every year for the next five years. In the next decade, more than twenty billion smart mobile devices will be connected to the Internet. This exponential growth is requiring new innovation throughout embedded devices and the supporting infrastructure to keep pace with the growing demand.

This talk will outline the evolution of embedded multicore processing solutions that are increasingly enabling the device and infrastructure markets. Topics covered will include the evolution of the network infrastructure, growth of multi-purpose embedded devices, increased trend towards heterogeneous system-on-chip (SOC) integration, balanced with the market realities of maintaining system development costs and energy efficiency. Continued innovation in every part of the value chain is needed in hardware design, software design, and in EDA tools. Key solutions and challenges for embedded multicore designs will be discussed as we move to advanced geometries and more highly integrated SOCs.

BIO:

Lisa Su is the senior vice president and general manager of networking and multimedia for Freescale Semiconductor.

Lisa joined Freescale in June 2007 as chief technology officer to lead Freescale's technology roadmap and global research and development (R&D) operations. She was named general manager of networking and multimedia in September 2008.

Prior to joining Freescale, Lisa was at International Business Machines Corporation (IBM), where she was vice president of the Semiconductor Research and Development Center and responsible for the strategic direction of IBM's silicon technologies, joint development alliances and semiconductor R&D operations. Lisa joined IBM in 1995 and held various engineering and business management positions including vice president of technology development and alliances in the IBM Systems and Technology Group and director of the PowerPC Product Line. Prior to IBM, Lisa was a Member of Technical Staff at Texas Instruments. She has extensive experience in the semiconductor industry leading technology innovation, microprocessor development and the launch of new products.

Lisa has authored or co-authored more than 40 technical publications and co-authored a book chapter on next-generation consumer electronics. She was named in MIT Technology Review's Top 100 Young Innovators in 2002 and was named Fellow of the IEEE in 2009. Lisa received bachelor's, master's and doctorate degrees in electrical engineering from the Massachusetts Institute of Technology.

GENERAL SESSION

Room: 20AB

OPENING REMARKS

Leon Stok - *48th DAC General Chair*

AWARDS PRESENTATIONS

KEYNOTE ADDRESS

MEGATRENDS DRIVING EMBEDDED MULTICORE INNOVATION

Lisa Su - *Vice President and General Manager of Networking and Multimedia for Freescale Semiconductor*

AWARDS

MARIE R. PISTILLI WOMEN IN EDA ACHIEVEMENT AWARD

Limor Fix - *Senior Principal Engineer, Director of Academic Programs and Research (ARP), Intel Corp., Hillsboro, OR*

For her significant contributions in helping women advance in the field of EDA technology.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIPS FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African-American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and a volunteer committee continues to administer the program for DAC. DAC normally funds a $4000 scholarship, renewable up to five years, to graduating high school seniors.

The 2011 recipient is:

Mario Morales

A. RICHARD NEWTON GRADUATE SCHOLARSHIPS

Each year the Design Automation Conference sponsors the A. Richard Newton Graduate Scholarship to support graduate research and study in Design Automation (EDA). Each scholarship is awarded directly to a University for the Faculty Investigator to expend in direct support of the project and students named in the application. The criteria are: the quality and applicability of the proposed research; the impact of the award on the EDA program at the institution; the academic credentials of the student(s); and financial need.

This year's scholarship goes to:

Advisor: Prof. Ayse K, Coskun - *Boston Univ., Boston, MA*

Student: Jie Meng - *Boston Univ., Boston, MA*

Project: 3D Systems for Low-Power High-Performance Computing

2010 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA

Sponsored by the EDA Consortium and IEEE Council on EDA

P.O. (Pat) Pistilli - *Chairman MP Associates, Inc.*

Pat Pistilli is honored for his pioneering the electronic design automation (EDA) industry and building the Design Automation Conference (DAC) as its premiere showcase and networking platform.

IEEE CEDA OUTSTANDING SERVICE CONTRIBUTION

For significant services as DAC General Chair 2010

Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

GENERAL SESSION

AWARDS

DONALD O. PEDERSON BEST PAPER AWARD FOR THE IEEE TRANSACTION ON CAD:

A. Singhee and R. A. Rutenbar

For Paper Titled: "Statistical Blockade: Very Fast Statistical Simulation and Modeling of Rare Circuit Events and Its Application to Memory Design,"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 8, pp. 1176-1189, August 2009.

ACM/IEEE A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

For pionieering work on technology mapping for FPGA that has made significant impact to the FPGA research community and industry.

"FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs"

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, January 1994, Vol. 13, Issue 1. Pages 1-12.

Authors:

Jason Cong - *Univ. of California, Los Angeles, CA*

Yuzheng "Eugene" Ding - *Xilinx Inc., Longmont, CO*

ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS (TODAES) 2011 BEST PAPER AWARD

For Paper Titled: "Cost minimization while satisfying hard/soft timing constraints for heterogeneous embedded systems"

TODAES Vol 14, No 2, Article 25, April 2009.

Authors: Meikang Qiu and Edwin H.-M. Sha

The Award recognizes the best paper published in the ACM Transactions on Design Automation of Electronic Systems in the time window from the April 2008 issue to the January 2011 issue.

SIGDA OUTSTANDING NEW FACULTY AWARD

Farinaz Koushanfar - *Rice Univ.*

For her pioneering research in the areas of secure, robust, and sustainable computing.

SIGDA OUTSTANDING PHD DISSERTATION AWARD

Nishant Patil – *Stanford Univ., Palo Alto, CA*

For the dissertation titled "Design and Fabrication of Imperfection-Immune Carbon Nanotube Digital VLSI Circuits," advised by Prof. Subhasish Mitra.

2011 STUDENT DESIGN CONTEST WINNING ENTRIES

A 90nm CMOS Data Flow Processor using Fine Grained DVS for Energy Efficient Operation from 0.3V to 1.2V

S. Arrabi, Y. Shakhsheer, K. Craig, S. Khanna, J. Lach, and B. H. Calhoun - *Univ. of Virginia*

A 1900MHz-Band GSM-Based Clock-Harvesting Receiver with -87dBm Sensitivity

Jonathan K. Brown and David D. Wentzloff - *Univ. of Michigan*

SRAM Dynamic Stability Characterization Using Pulsed Word-lines in 45nm CMOS

Seng Oon Toh and Borivoje Nikolic - *Univ. of California*

Design and Implementation of Centip3De, a 7-layer Many-Core System

David Fick, Ronald G. Dreslinski, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wiekowski, Gregory Chen, Trevor Mudge, Dennis Sylvester, and David Blaauw - *Univ. of Michigan*

A Flexible Wireless Receiver System with a 7b 21 MS/s Filtering SAR ADC

David T. Lin, Li Li, John Bell, Ming-Hao Wang and Michael P. Flynn - *Univ. of Michigan*

Augmented Reality Headset based on a Heterogeneous Multi-core Object Recognition Chip

Seungjin Lee, Jinwook Oh, Junyoung Park, Joonsoo Kwon, and Hoi-Jun Yoo - *KAIST*

A 0.9-V 11-bit 25-MS/s 0.58-mW Binary-Search SAR ADC in 90-nm CMOS

Ying-Zu Lin, Ya-Ting Shyu, Guan-Ying Huang, Chun-Cheng Liu and Soon-Jyh Chang - *National Cheng Kung Univ.*

A Video Stabilization System with Background Motion Estimation and Smoothing for Digital Camera

Chih-Lun Fang, Hui-Min Chuang and Tsung-Han Tsai - *National Central Univ.*

WEDNESDAY KEYNOTE

June 8

11:00am - 12:00pm **Room: 20AB**

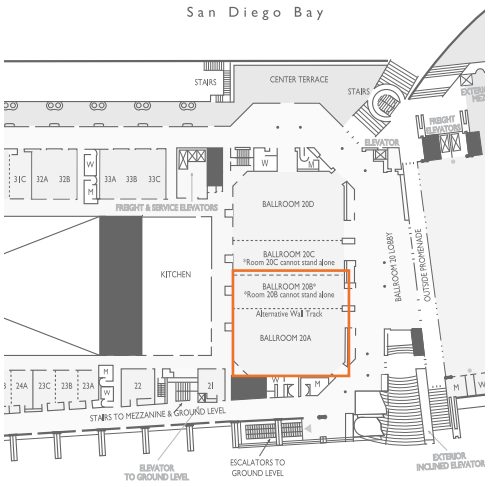
THE IMMINENT EDA TRANSFORMATION

GADI SINGER

Intel Corp., Santa Clara, CA

SUMMARY:

The EDA industry faces a substantial shift. Electronic systems are going through fundamental and rapid change in domains ranging from TVs and in-vehicle devices to phones, tablets, and even PCs. These new systems require unprecedented connectivity, hardware and software complexity, and application and user interactions. To meet these challenges, the EDA industry must evolve and expand quickly to enable highly interdependent silicon, software, system, and experience solutions. The EDA industry's current offering needs to be reassessed, and the scope of the industry's capabilities and environments needs to encompass exploration, design, verification, and debug across the complete hardware and software stack. This keynote will highlight opportunities for innovation and the changes necessary to support this brisk evolution and value creation in electronic systems.



BIO:

Gadi Singer is vice president of the Intel Architecture Group and General Manager, SOC Enabling Group for Intel Corporation. The SOC Enabling Group is responsible for delivering central building blocks and driving Intel's SOC silicon design and software development capabilities focusing on fast turnaround time and modularity practices. Singer joined Intel in 1983, holding a variety of senior technical and management positions. He was appointed VP in 1999 and CTO of Intel Communications Group in 2004, among other accomplishments.

From 2005 through 2007, Singer served as General Manager of the Ultra Mobility Group. Among his prior roles, Singer was GM of Intel's Design Technology Division, co-GM of the IA-64 Processor Division and GM of Enterprise Processors Division. Singer received three Intel Achievement Awards for his technical contributions. He was Chairman of EDA Industry Council from 1997 to 1999. Singer is alumnus of the Technion, Israel.

THURSDAY KEYNOTE

June 9

11:00am - 12:00pm **Room: 20AB**

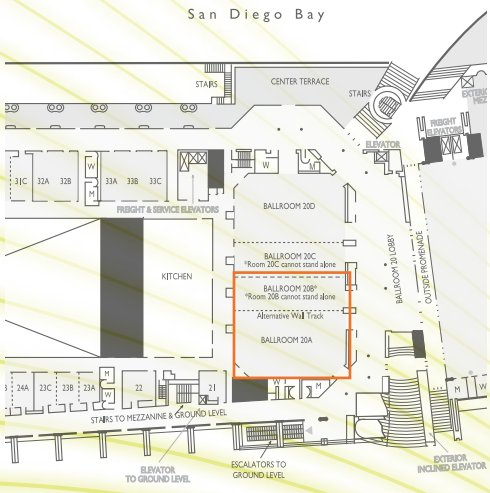
COGNITIVE COMPUTING: NEUROSCIENCE, SUPERCOMPUTING, NANOTECHNOLOGY

DHARMENDRA S. MODHA

IBM Research - Almaden, San Jose, CA

SUMMARY:

The ultimate goal of the DARPA SyNAPSE project is to build brain-like cognitive computing chips that scale to human cortex by moving beyond the von Neumann architecture and become the brains behind IBM's Smarter Planet vision. The project leverages nanotechnology, supercomputing, and neuroscience and is a collaboration of four universities (Cornell, Columbia, Wisconsin-Madison, and UC Merced) and five IBM sites (Almaden, Yorktown, EFK, BTV, and IRL).



BIO:

Dr. Dharmendra S. Modha is founding manager of the Cognitive Computing group at IBM's Almaden Research Center. Currently, he is the Principal Investigator for DARPA SyNAPSE team of IBM Research - Almaden, IBM Research - Watson, University of Wisconsin-Madison, Cornell University, Columbia University, and University of California at Merced. Most recently, his group performed cortical simulations at scale of cat cerebral cortex (1 billion neurons, 10 trillion synapses) only 100x slower than real-time on a 147,456 processor BlueGene/P supercomputer. This work received the 2009 ACM's Gordon Bell Prize. In 2010, his group compiled, visualized, and analyzed the largest long-distance network currently in existence of the Macaque monkey brain.

His research has had significant practical impact on IBM's businesses. At IBM, he has won the Pat Goldberg Memorial Best Paper award (twice), an Outstanding Innovation Award, an Outstanding Technical Achievement Award, and Communication Systems Best Paper Award. He holds 29 US patents, and is currently an IBM Master Inventor. In 2010, he was elected to the IBM Academy of Technology.

He has authored over 50 publications in international journals and conferences. He is a Fellow of IEEE and a member of AAAS, ACM, and SfN.

Dr. Modha holds a B.Tech. in Computer Science and Engineering from IIT Bombay and a Ph. D. in Electrical and Computer Engineering from UCSD.

MANAGEMENT DAY

Sponsored by: SYNOPSYS®

Additional Registration Fees apply

Tuesday, June 7 10:30am - 6:30pm Room: 32AB

Organizer:

Yervant Zorian - *Synopsys, Inc., Fremont, CA*

The DAC 2011 Management Day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

Today's complex SOCs require different types of optimizations and the adoption of emerging solutions to meet such requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. Also, moving to new semiconductor technology nodes, such as 22nm or 28nm, can significantly affect the choices of suppliers. The Management Day sessions will discuss these changing needs and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options for flows, methodologies, and suppliers.

The Management Day is comprised of three sessions. The first two sessions will feature presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers, foundries, and fabless companies. Senior managers of today's most complex nanometer chips – from Intel, Samsung, Global Foundries, ST Microelectronics, Qualcomm, and other leading companies – will discuss the latest and emerging solutions, along with their economic impact. The third session will be a panel to involve the presenters and the audience in an open brainstorming discussion.

SESSION 1: DECISION MAKING FOR COMPLEX ICS

10:30am - 12:00pm

Session Chair:

Rich Valera - *Needham & Co., San Francisco, CA*

Moving to new semiconductor technology nodes for complex ICs can significantly affect the choices of design flow, methodologies and suppliers. This session will cover the challenges of complex chip design and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options. This session feature presentations by managers representing independent device manufacturers (IDMs), fab-less ASIC providers, and fabless companies.

Speakers:

Sunil Shenoy - *Vice President, Digital Enterprise Group, Intel Corp., Hillsboro, OR*
Kee Sup Kim - *Vice President Design Technology, Samsung, Yongin-City, Republic of Korea*
Naveed Sherwani - *President, Co-founder & CEO, Open-Silicon Inc., Milpitas, CA*

SESSION 2: TRADE-OFFS AND CHOICES FOR EMERGING SOCS

2:00 - 4:00pm

Session Chair:

Brian Fuller - *EE Times*

Today's emerging SOCs require multiple types of optimizations and the adoption of advanced solutions to meet stringent design requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. This session will feature senior managers of today's most complex nanometer chips.

Speakers:

Philippe Magarshack - *R&D Group Vice President & GM, ST Microelectronics, Crolles, France*
Kevork Keechichian - *Vice President Engineering, Qualcomm CDMA Technologies, San Diego, CA*
Robert Madge - *Director, Design Enabled Manufacturing, GLOBALFOUNDRIES, Milpitas, CA*
Magdy Abadir, Raj Raina - *Director, Design Automation & Vendor Relations, Freescale Semiconductor, Austin, TX*

SESSION 3: PANEL: CLOUD COMPUTING (HELD NEXT DOOR IN ROOM 33AB)

4:00 - 6:30pm

Session Chair:

Raul Camposano - *Physware, Inc., Mountain View, CA*

Session Organizer:

Andreas Kuehlmann - *Coverity, Inc., San Francisco, CA*

This panel is preceded by a 30 minute tutorial on effective use of the cloud by Amazon's Peter DeSantis.

Cloud computing is THE buzz word today in the software industry. So how and when will cloud computing affect EDA and IC design? Immediate concerns looming on the horizon are security, the transfer of large data sets, and licensing models. This panel, representing a broad set of design and EDA constituents, will examine cloud computing's many implications for the IC design ecosystem.

Speakers:

Peter DeSantis - *Amazon.com, Inc., Seattle, WA*
John Chilton - *Synopsys, Inc., Mountain View, CA*
John Bruggeman - *Cadence Design Systems, Inc., San Jose, CA*
Greg Gottesman - *Madrona Venture Group, Inc., Seattle, WA*
Mojy Chian - *GLOBALFOUNDRIES, Milpitas, CA*
Carl Anderson - *IBM Corp., Austin, TX*

ESS EXECUTIVE DAY

Wednesday, June 8 9:00am - 5:30pm Room: 32AB

Organizer:
Yervant Zorian - *Synopsys, Inc., Fremont, CA*

New for this year's DAC is the focus on Embedded Systems and Software (ESS). The hardware and software design convergence and interdependence in today's complex embedded systems continues to increase. The ESS Executive Day provides managers with timely information to help them make decisions where business and technology in this increasingly important domain intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

IC design engineers, embedded systems designers, embedded software and hardware IP providers, IP integrators, FPGA designers, investors, foundry reps, and the media will be on hand in this new forum to hear from market leaders and to network with each other. The ESS Executive Day is a day-long track of sessions dedicated to bringing industry stakeholders together in one room to shed light on where system design is headed. The day is comprised of presentations from leading industry executives representing the above sectors.

Presenters will focus on optimization of embedded and application-domain specific operating systems, system architecture for future embedded products, application-specific architectures based on embedded processors and technical/business decision making by program developers. They will cover the state-of-the-art solutions for embedded software and systems and complex chips. Such solutions often require tight collaboration between diverse players in this ecosystem. Moving to new levels of complexity can significantly affect the choices of suppliers. The new ESS Executive Day provides a unique opportunity to foster discussions that address all aspects of the embedded development ecosystem.

SESSION 1:

9:00 - 10:30am

Speakers:
Ivo Bolsens - *Senior VP and CTO, Xilinx, Inc., San Jose, CA*
Misha Burich - *Senior VP Research and Development, Altera Corp., San Jose, CA*
John Goodenough - VP Design Technology, *ARM, Ltd., Cambridge, United Kingdom*
Joachim Kunkel - *Senior VP, Synopsys, Mountain View, CA*

SESSION 2:

2:00 - 3:30pm

Speakers:
John Bruggeman - *Chief Marketing Officer, Cadence Design Systems, Inc., San Jose, CA*
Sami Issa - *Executive Director, Advanced Technology Investment Company, LLC, United Arab Emirates*
Gabriele Saucier - *President and CEO, Design and Reuse, Grenoble, France*

SESSION 3:

4:00 - 5:30pm

Speakers:
Simon Bloch - *VP and General Manager, Mentor Graphics Corp., San Jose, CA*
Ron Collett - *President and CEO, Numetrics, Cupertino, CA*
Grant Martin - *Cheif Scientist, Tensilica, Inc., Santa Clara, CA*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 10:30am - 12:00pm | Embedded Systems and Software | Room: 33ABC

1 PANEL: HACKERS AND ATTACKERS: HOW SAFE IS YOUR EMBEDDED DESIGN?

Chair(s):
Ted Vucurevich - *Slightly Sharp Enterprises, Atherton, CA*

Organizer(s):
Farinaz Koushanfar - *Rice Univ., Houston, TX*
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

Speaker(s):
Divya Aröra - *Intel Corp., Santa Clara, CA*
Hovav Shacham - *Univ. of California at San Diego, La Jolla, CA*
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*
Jesus Molina - *Fujitsu, Santa Clara, CA*
Kevin Fu - *Univ. of Massachusetts, Amherst, MA*

We daily entrust embedded devices with our most sensitive information and literally our lives - from smart phones and online banking to critical medical devices such as pacemakers. All this makes embedded systems a delicious target for online attacks and malicious code hackers. Come hear embedded security experts discuss both the growing risks and the emerging tools and methodologies for embedded designers.

Tuesday, June 7 10:30am - 12:00pm | Embedded Systems and Software | Room: 29AB

2 SPECIAL SESSION: DESIGN METHODS AND TRENDS FOR AUTOMOTIVE ARCHITECTURES

Chair(s):
Marco di Natale - *Scuola Superiore Sant'Anna, Pisa, Italy*
Jörg Henkel - *Karlsruher Institut für Technologie, Karlsruhe, Germany*

Organizer(s):
Jürgen Teich - *Friedrich-Alexander-Universität Erlangen-Nürnberg, Nuremberg, Germany*
Samarjit Chakraborty - *Technische Univ. München, Munich, Germany*

How many embedded processors can you find in your BMW 7 series or in your Tahoe Hybrid? How many millions of lines of code do these embedded processors run? How do these processors communicate? The behavior of today's automobiles, from engine to climate control, is governed by embedded electronics. Current and future requirements for distributed driver assistance and infotainment applications overstrain classic E/E (Electrical/Electronics) architectures and, in particular, their communication infrastructure. This session presents opportune design methods and trends for future automotive network architectures. The talks in this session present novel design concepts for heterogeneous automotive networks that include Ethernet and FlexRay with a focus on challenges, constraints, and realizations.

2.1 Application and Realization of Gateways Between Conventional Automotive and IP/Ethernet-Based Networks
Josef Nöbauer, Helge Zinner, Thomas Gallner - *Continental Automotive GmbH, Regensburg, Germany*
Jochen Seitz - *Technische Universität Ilmenau, Ilmenau, Germany*
Thomas Waas - *Hochschule Regensburg, Regensburg, Germany*

2.2 Challenges in a Future IP/Ethernet-Based, In-Car Network for Real-Time Applications
Hyung-Taek Lim, Daniel Herrscher - *BMW Group Research and Technology, Munich, Germany*
Lars Völker - *BMW Group, Munich, Germany*

2.3 Rigorous Model-Based Design and Verification Flow for In-Vehicle Software
S. Ramesh, Ambar Gadkari - *India Science Lab., General Motors Global R&D, Bangalore, India*

Tuesday, June 7 10:30am - 12:00pm | Embedded Systems and Software | Room: 29CD

3 PERFORMANCE AND RELIABILITY OF FLASH MEMORY SYSTEMS

Chair(s):
Chang-Gun Lee - *Seoul National Univ., Seoul, Republic of Korea*

This session presents recent advances in performance and reliability enhancement for flash memory systems. The first paper proposes several novel techniques for improving performance of multi-level cell flash memory. The second paper proposes an approach to write buffer management for improving performance by balancing the two flash-translation-layer strategies of logging and plugging. The third paper presents a version-based strategy for enhancing reliability of flash memory while minimizing the overhead in memory space. The fourth paper characterizes the behavior of flash memories during power failure, which can be a base for future research on enhancing power-related reliability of flash memory systems.

3.1 MNFTL: An Efficient Flash Translation Layer for MLC NAND Flash Memory Storage Systems
Zhiwei Qin, Yi Wang, Duo Liu, **Zili Shao** - *The Hong Kong Polytechnic Univ., Kowloon, Hong Kong*
Yong Guan - *Capital Normal Univ., Beijing, China*

3.2 Plugging Versus Logging: A New Approach to Write Buffer Management for Solid-State Disks
Li-Pin Chang, You-Chiuan Su - *National Chiao Tung Univ., Hsinchu, Taiwan*

3.3 A Version-Based Strategy for Reliability Enhancement of Flash File Systems
Pei-Han Hsu, **Po-Chun Huang**, Tei-Wei Kuo - *National Taiwan Univ., Taipei, Taiwan*
Yuan-Hao Chang - *National Taipei Univ. of Technology, Taipei, Taiwan*
David Hung-Chang Du - *Univ. of Minnesota, Minneapolis, MN*

3.4 Understanding the Impact of Power Loss on Flash Memory
Hung-Wei Tseng, Laura M. Grupp, Steven J. Swanson - *Univ. of California at San Diego, La Jolla, CA*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 10:30am - 12:00pm | **Low-Power Design** | **Room: 30C**

4 SYSTEM-LEVEL POWER MANAGEMENT

Chair(s):
Daniel Gajski - *Univ. of California, Irvine, CA*

The best opportunity for power savings is at the system level. The papers in this session focus on system-level power management techniques for creating power-efficient designs. The first paper focuses on a system workload predictor model for reducing energy consumption, and is followed by a paper describing an integrated power methodology for analyzing multicore SOC designs. The third paper in the session outlines a dynamic voltage scaling technique for reducing the power usage for an OLED display while still providing high quality images. The session concludes with a paper on a novel DRAM/PRAM approach for memory.

4.1 Deriving a Near-Optimal Power Management Policy Using Model-Free Reinforcement Learning and Bayesian Classification
Yanzhi Wang, **Qing Xie**, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Ahmed C. Ammari - *INSAT, Tunis Cedex, Tunisia*

4.2 Power Depot: Integrating IP-Based Power Modeling with ESL Power Analysis for Multicore SOC Designs
Chen-Wei Hsu, Jia-Lu Liao, **Chia-Chien Weng**, Shi-Yu Huang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Shan-Chien Fang - *TinnoTek Inc., Hsinchu, Taiwan*
Wen-Tsan Hsieh, Jen-Chieh Yeh - *Industrial Technology Research Institute, Hsinchu, Taiwan*

4.3 Dynamic Voltage Scaling of OLED Displays
Donghwa Shin, Younghyun Kim, Naehyuck Chang - *Seoul National Univ., Seoul, Republic of Korea*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

4.4 Power Management of Hybrid DRAM/PRAM-Based Main Memory
Hyun Sun Park, Sungjoo Yoo, Sunggu Lee - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

Tuesday, June 7 10:30am - 12:00pm | **DFM and the Manufacturing Interface** | **Room: 31AB**

5 DESIGN FOR MANUFACTURABILITY

Chair(s):
Charles Chiang - *Synopsys, Inc., Mountain View, CA*

This session looks into recent DFM topics. The first paper evaluates the importance of design rules. The second paper looks into self-aligned double-patterning decomposition along with hotspot detection. The third paper develops variability models for standard cells. The final paper develops a synthesis methodology for layouts with regular fabrics.

5.1 To DFM or Not to DFM?
Wing Chiu Tam, Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

5.2 Self-Aligned Double-Patterning Decomposition for Overlay Minimization and Hot Spot Detection
Hongbo Zhang, Yuelin Du, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Rasit O. Topaloglu - *GLOBALFOUNDRIES, Santa Clara, CA*

5.3 Statistical Characterization of Standard Cells Using Design of Experiments with Response Surface Modeling
Miguel Miranda, Philippe Roussel, Lucas Brusamarello - *IMEC, Leuven, Belgium*
Gilson Wirth - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

5.4 Physical Synthesis onto a Layout Fabric with Regular Diffusion and Polysilicon Geometries
Nikolai Ryzhenko, Steven Burns - *Intel Corp., Hillsboro, OR*

Tuesday, June 7 10:30am - 12:00pm | **Low-Power Design** | **Room: 31C**

6 THERMAL MANAGEMENT AND MODELING FOR INTEGRATED CIRCUITS

Chair(s):
Ayse Coskun - *Boston Univ., Boston, MA*

The papers in this session address thermal considerations for integrated circuits. The session starts with two papers that present novel dynamic thermal management techniques for microprocessors. The first paper presents a technique for inserting idle cycles for thermal control. The second paper uses a machine-learning based technique for voltage and frequency control that is effective for multimedia applications. The third paper presents a technique to improve power models using post-silicon IR analysis, and the last paper presents a computationally efficient metric that correlates with temperature and is used for floorplan optimization.

6.1 Dimetrodon: Processor-Level Preventive Thermal Management via Idle Cycle Injection
Peter D. Bailis, Sanjay Gandhi, David Brooks, Margo Seltzer - *Harvard Univ., Cambridge, MA*
Vijay Janapa Reddi - *Advanced Micro Devices, Inc., Cambridge, MA*

6.2 Dynamic Thermal Management for Multimedia Applications Using Machine Learning
Yang Ge, Qinru Qiu - *SUNY Binghamton, Vestal, NY*

6.3 Improved Post-Silicon Power Modeling Using AC Lock-In Techniques
Abdullah N. Nowroz, Sherief Reda - *Brown Univ., Providence, RI*
Gary Woods - *Rice Univ., Houston, TX*

6.4 Thermal Signature: A Simple Yet Accurate Thermal Index for Floorplan Optimization
Jaeha Kung, Inhak Han, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 2:00 - 3:30pm | **Low-Power Design** | **Room: 33ABC**

7 PANEL: CRYSTAL BALL ON LOW POWER: LIMITING TRENDS AND STRATEGIC SOLUTIONS

Chair(s):
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

Organizer(s):
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

Speaker(s):
Jan Rabaey - *Univ. of California, Berkeley, CA*
Ed Huijbregts - *Magma Design Automation, Inc., Eindhoven, The Netherlands*
S Balajee - *Texas Instruments, Inc., Bangalore, India*
K.S. Kim - *Samsung, Yongin, KR*
Vivek De - *Intel Corp., Hillsboro, OR*
Matt Severson - *Qualcomm, Inc., San Diego, CA*
Wilfried Haensch - *IBM T.J. Watson Research Ctr., Yorktown Heights, NY*

This panel addresses the entire low-power picture to determine who ultimately is responsible for meeting the low-power system needs. Device engineers could once again save the day. Or, maybe, design and EDA must step up and shoulder the burden. Others insist that system architecture and software solutions will ultimately solve the looming power crisis. The panel will shed light on key technology limits, system needs, and potential solutions.

Tuesday, June 7 2:00 - 3:30pm | **Bio Design Automation** | **Room: 29AB**

8 SPECIAL SESSION: DESIGN AND SYNTHESIS OF BIOLOGICAL CIRCUITS

Chair(s):
Douglas Densmore - *Boston Univ., Boston, MA*
Mark Horowitz - *Stanford Univ., Stanford, CA*

Organizer(s):
Smita Krishnaswamy - *Columbia Univ., New York, NY*
Xiling Shen - *Cornell Univ., Ithaca, NY*

With the growing complexity of synthetic biological circuits, robust and systematic methods are needed for design and test. Leveraging lessons learned from the semiconductor and design automation industries, synthetic biologists are starting to adopt computer aided design and verification software with some success. However, due to the great challenges associated with designing synthetic biological circuits, this nascent approach has to address many problems not present in electronic circuits. In this session, three leading synthetic biologists will share with us how they have developed software tools to help design and verify their synthetic circuits, the unique challenges they faced, and their insight into the next generation of tools for synthetic biology.

8.1 Scalable Parts Families, Context, and Computational Design for Gene Expression Engineering
Adam Arkin - *Univ. of California, Berkeley, CA*

8.2 Gene and Cellular Circuit Design
Chris Voigt - *Univ. of California, San Francisco, CA*

8.3 A Verifying Compiler for DNA Chemical Reaction Networks
Erik Winfree, Seung Woo Shin - *California Institute of Technology, Pasadena, CA*

Tuesday, June 7 2:00 - 3:30pm | **Embedded Systems and Software** | **Room: 29CD**

9 SWEET STREAMS, EMBEDDED IN MULTICORES

Chair(s):
Luca Carloni - *Columbia Univ., New York, NY*

This session begins with a presentation of work on modeling streaming applications with runtime parameters through Parameterized Polyhedral Process Networks including an evaluation of the overhead introduced by parameterization. We will then hear about work on compiling stream programs onto multicore systems with scratchpad memory through retiming that maximizes throughput under memory constraints. The session continues with work on improving GPGPU application performance through memory access analysis. The final presentation is on improving soft error-aware, low-power scheduling through recursive Monte Carlo state space exploration of task execution times.

9.1 Modeling Adaptive Streaming Applications with Parameterized Polyhedral Process Networks
Jiali Teddy Zhai, Hristo Nikolov, Todor Stefanov - *Leiden Univ., Leiden, The Netherlands*

9.2 Compilation of Stream Programs onto Scratchpad Memory-Based Embedded Multicore Processors Through Retiming
Weijia Che, Karam S. Chatha - *Arizona State Univ., Tempe, AZ*

9.3 CuMAPz: A Tool to Analyze Memory Access Patterns in CUDA
Yooseong Kim, Aviral Shrivastava - *Arizona State Univ., Tempe, AZ*

9.4 SEAL: Soft Error-Aware, Low-Power Scheduling by Monte Carlo State Space Under the Influence of Stochastic Spatial and Temporal Dependencies
Nabeel Iqbal, Muhammad Adnan Siddique, Jörg Henkel - *Karlsruher Institut für Technologie, Karlsruhe, Germany*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 2:00 - 3:30pm | **Synthesis and FPGA** | **Room: 30C**

10 LATE FLOW OPTIMIZATION AND RECTIFICATION

Chair(s):
Andreas Kuehlmann - *Coverity, Inc., San Francisco, CA*

Initial synthesis is rarely the final implementation. In this session, we examine ways that designs can be improved or fixed either late in the flow, or after fabrication. The first paper presents a unifying methodology for fixing both timing and functional issues. The second paper uses multiple passes of partial rectification to fix multiple errors efficiently. The third paper presents theoretical complexity results on the multi-domain clock skew scheduling problem, as well as improved heuristics. The final paper examines techniques to optimize circuits utilizing timing speculation by reducing timing-suspicious flip flops and improving the padding of short paths.

10.1 Simultaneous Functional and Timing ECO
Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Hua-Yu Chang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

10.2 Interpolation-Based Incremental ECO Synthesis for Multi-Error Logic Rectification
Kai-Fu Tang, Chi-An Wu, Po-Kai Huang, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

10.3 Optimal Multi-Domain Clock Skew Scheduling
Li Li, **Yinghai Lu**, Hai Zhou - *Northwestern Univ., Evanston, IL*

10.4 Resynthesis for Cost-Efficient, Circuit-Level Timing Speculation
Yuxi Liu, Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

Tuesday, June 7 2:00 - 3:30pm | **Physical Design** | **Room: 31AB**

11 ROUTING REVIVED

Chair(s):
Li Zhuo - *IBM Corp., Austin, TX*

This session proposes new techniques in routing. The first paper presents an optimal algorithm for constructing rectilinear Steiner minimum trees with rectilinear-shaped obstacles. The second paper deals with complex pin access during detailed routing. The third paper is on optimal layer assignment for PCB escape routing, and the last paper proposes a distributed algorithm for layout processing.

11.1 An Exact Algorithm for the Construction of Rectilinear Steiner Minimum Trees Among Complex Obstacles
Tao Huang, Evangeline F. Y. Young - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

11.2 Gridless Pin Access in Detailed Routing
Tim Nieberg - *Universität Bonn, Bonn, Germany*

11.3 An Optimal Algorithm for Layer Assignment of Bus Escape Routing on PCBs
Qiang Ma, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Evangeline F. Y. Young - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

11.4 A Distributed Algorithm for Layout Geometry Operations
Kai-Ti Hsu, Yu-Chuan Pi, Tsung-Yi Ho - *National Cheng Kung Univ., Tainan City, Taiwan*
Subarna Sinha, Charles Chiang - *Synopsys, Inc., Mountain View, CA*

Tuesday, June 7 2:00 - 3:30pm | **Interconnect and Reliability** | **Room: 31C**

12 IT'S ALL IN THE MODELS...

Chair(s):
Eric Keiter - *Sandia National Laboratories, Albuquerque, NM*

Papers in this session emphasize the importance of proper modeling of the physical properties of systems. Good models capture relevant behavior accurately and can be efficiently generated and evaluated, enabling analysis of performance, yield, or reliability.

The first three papers focus on model approaches to address manufacturing and operating conditions or process variations. The papers cover issues ranging from mechanical reliability, modeling spatial variations on an IC, and improving failure rate estimation. The final two papers address the efficiency of model generation and evaluation by employing careful statistical analysis as well as appropriate compressed representations.

12.1 TSV Stress-Aware, Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC
Sung Kyu Lim, **Moongon Jung** - *Georgia Institute of Technology, Atlanta, GA*
Joydeep Mitra, David Z. Pan - *Univ. of Texas, Austin, TX*

12.2 Hybrid Modeling of Non-Stationary Process Variations
Eva Dyer, Mehrdad Majzoobi, Farinaz Koushanfar - *Rice Univ., Houston, TX*

12.3 Efficient SRAM Failure Rate Prediction via Gibbs Sampling
Xin Li, Changdao Dong - *Carnegie Mellon Univ., Pittsburgh, PA*

12.4 Direct Matrix Solution of Linear Complexity for Surface Integral Equation-Based Impedance Extraction of High Bandwidth Interconnects
Wenwen Chai, Dan Jiao - *Purdue Univ., West Lafayette, IN*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 4:00 - 6:00pm | Emerging Technologies | Room: 33ABC

13 PANEL: CLOUD COMPUTING AND EDA FORECAST: SUNNY SKIES OR STORM CLOUDS AHEAD?

Chair(s):
Raul Camposano - *Physware, Inc., Mountain View, CA*

Organizer(s):
Andreas Kuehlmann - *Coverity, Inc., San Francisco, CA*

Speaker(s):
Peter DeSantis - *Amazon.com, Inc., Seattle, WA*
John Chilton - *Synopsys, Inc., Mountain View, CA*
John Bruggeman - *Cadence Design Systems, Inc., San Jose, CA*
Greg Gottesman - *Madrona Venture Group, Inc., Seattle, WA*
Mojy Chian - *GLOBALFOUNDRIES, Milpitas, CA*
Carl Anderson - *IBM Corp., Austin, TX*

This panel is preceded by a 30 minute tutorial on effective us of the cloud by Amazon's Peter DeSantis.

Cloud computing is THE buzz word today in the software industry. So how and when will cloud computing affect EDA and IC design? Immediate concerns looming on the horizon are security, the transfer of large data sets, and licensing models. This panel, representing a broad set of design and EDA constituents, will examine cloud computing's many implications for the IC design ecosystem.

Tuesday, June 7 4:00 - 6:00pm | Emerging Technologies | Room: 29AB

14 SPECIAL SESSION: KILLER APPS FOR 3-D ICS?

Chair(s):
Lei He - *Univ. of California, Los Angeles, CA*

Organizer(s):
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

3-D IC technology has promised a great deal for several years - but is it ready to move from being the technology of tomorrow to that of today? The NRE costs associated with 3-D design, manufacturing, and test are steep, and cannot be justified without killer apps that provide the appropriate ROI. This session features four talks from industry experts on their view of apps that will help move 3-D towards the mainstream. The topics covered in this session include design challenges and opportunities, processor/memory issues, and heterogeneous 3-D integration, including systems that integrate optical and RF interconnects.

14.1 Design, CAD, and Technology Challenges for Future Processors: 3-D Perspectives
Jeff Burns, Gary Carpenter, Eren Kursun, Ruchir Puri, **James Warnock**, Michael Scheuermann - *IBM Corp., Yorktown Hts, NY*

14.2 3-D Heterogeneous System Integration: Application Driver for 3-D Technology Development
Eric Beyne, Pol Marchal, Geert Van Der Plas - *IMEC, Leuven, Belgium*

14.3 3D Integration for Energy Efficient System Design
Shekhar Borkar - *Intel Corp., Hillsboro, OR*

14.4 Applications Driving 3-D Integration and Corresponding Manufacturing Challenges
Rasit Topaloglu - *GLOBALFOUNDRIES, Milpitas, CA*

Tuesday, June 7 4:00 - 6:00pm | Embedded Systems and Software | Room: 29CD

15 TOWARDS EMBEDDED SYSTEMS WE CAN TRUST: FROM MODELS TO GATES

Chair(s):
Nachiketh Potlapally - *Intel Corp., Princeton, NJ*

This session deals with the trustworthiness of embedded systems from abstract models down to gates. The first paper presents a novel test-case generation technique using formal concept analysis. The second paper presents a design flow for software to mitigate the power side channel. The third paper presents a simulation for estimating the impact of TPM on the performance of applications. The fourth paper proposes a prototype architecture for a low-cost and fast, public, and physically unclonable function. The next paper shows how variable supply voltage techniques can be used to detect three types of IC trojan attacks. The final paper demonstrates the application of gate-level information flow tracking to provide a method for testing information flows in two common bus protocols.

15.1 Test-Case Generation for Embedded Simulink via Formal Concept Analysis
Nannan He, Daniel Kroening - *Oxford Univ., Oxford, United Kingdom*
Philipp Ruemmer - *Uppsala Univ., Uppsala, Sweden*

15.2 A First Step Towards Automatic Application of Power Analysis Countermeasures
Ali Galip Bayrak, Paolo Ienne - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Francesco Regazzoni, Francois-Xavier Standaert - *Univ. Catholiqué de Louvain, Baaschtnech, Belgium*
Philip Brisk - *Univ. of California, Riverside, CA*

15.3 TPM-SIM: A Framework for Performance Evaluation of Trusted Platform Modules
Jared Schmitz, Jason Loew, Jesse Elwell, Dmitry Ponomarev, Nael Abu-Ghazaleh - *SUNY Binghamton, Binghamton, NY*

15.4 Differential Public, Physically Unclonable Functions: Architecture and Applications
Miodrag Potkonjak, Sheng Wei, Saro Meguerdichian, Ani Nahapetian - *Univ. of California, Los Angeles, CA*

15.5 Integrated Circuit Security Techniques Using Variable Supply Voltage
Miodrag Potkonjak, **Sheng Wei** - *Univ. of California, Los Angeles, CA*

15.6 Information Flow Isolation in I2C and USB
Jason Oberg, Ali U. Irturk, Ryan Kastner - *Univ. of California at San Diego, La Jolla, CA*
Wei Hu - *Northwestern Polytechnical Univ., Xian, China*
Mohit Tiwari, Timothy Sherwood - *Univ. of California, Santa Barbara, CA*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Tuesday, June 7 4:00 - 6:00pm | **System-Level Design** | **Room: 30C**

16 SPECIAL SESSION: EMBEDDED MULTIPROCESSOR SOFTWARE SYNTHESIS

Chair(s):
Peter Marwedel - *Technische Univ. Dortmund, Dortmund, Germany*
Daniel Gajski - *Univ. of California, Irvine, CA*

Organizer(s):
Andreas Gerstlauer - *Univ. of Texas, Austin, TX*
Christian Haubelt - *Friedrich-Alexander-Universität Erlangen-Nürnberg, Nuremberg, Germany*

Future embedded systems will consist of tens to hundreds of heterogeneous programmable cores. How do we optimally program them? The synthesis of optimized software implementations that respect tight constraints imposed by operating environments from high-level, abstract input models becomes very attractive. This session will present state-of-the-art approaches for embedded multi-processor software development, with topics ranging from the search for novel temporal abstractions and programming models to complete environments for automatic synthesis of efficient and performance-, power- and temperature-optimized software across heterogeneous SOCs, including perspectives from both practitioners in industry as well as academic researchers.

16.1 CIRUS: A Scalable Modular Architecture for Reusable Drivers
Bratin Saha - *Intel Corp., Santa Clara, CA*

16.2 Programming Challenges and Solutions for Multiprocessor SOCs: An Industrial Perspective
Pierre G. Paulin - *STMicroelectronics, Ottawa, ON, Canada*

16.3 Thermal-Aware System Analysis and Software Synthesis for Embedded Multiprocessors
Lothar Thiele, Lars Schor, Hoeseok Yang, Iuliana Bacivarov - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*

16.4 Temporal Isolation on Multiprocessing Architectures
Dai Bui, **Edward A. Lee**, Isaac Liu, Jan Reineke - *Univ. of California, Berkeley, CA*
Hiren Patel - *Univ. of Waterloo, Waterloo, ON, Canada*

Tuesday, June 7 4:00 - 6:00pm | **General Interest** | **Room: 31AB**

17 WILD AND CRAZY IDEAS

Chair(s):
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The WACI session showcases wild and crazy, thought-provoking ideas and is intended to promote wild and crazy discussion and debate. This year's presentations include applications of EDA to social networks and internet search, "true" 3-D architectures with vertical transistors, orchestrated flow analysis to benefit ever-changing design teams, binary translation for acceleration on-the-fly, using device aging to improve circuit security, and energy-efficient computing on unreliable platforms. We expect the wild and crazy questions that make the WACI experience complete; the WACIest presentation and the WACIest question will be appropriately recognized!

17.1 Physics-Based, Field-Theoretic Design Automation Tools for Social Networks and Web Search
Vikram Jandhyala - *Univ. of Washington, Seattle, WA*

17.2 Can We Go Towards True 3-D Architectures?
Pierre-Emmanuel Gaillardon, Haykel Ben-Jamaa, Paul-Henry Morel, Jean-Philippe Noël, Fabien Clermidy - *CEA-Leti, Grenoble, France*
Ian O'Connor - *École Centrale de Lyon, Lyon, France*

17.3 Orchestrated Multi-Level Information Flow Analysis to Understand SOCs
Görschwin Fey - *Univ. Bremen, Bremen, Germany*

17.4 Dynamic Binary Translation to a Reconfigurable Target for On-the-Fly Acceleration
Phillip J. Kinsman, Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

17.5 Device Aging-Based Physically Unclonable Functions
Saro Meguerdichian, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

17.6 Significance-Driven Computation On Next-Generation Unreliable Platforms
Georgios Karakonstantis - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Nikolaos Bellas, Christos Antonopoulos, Georgios Tziatzaoulis - *Univ. of Thessaly, Volos, Greece*
Vaibhav Gupta, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

Tuesday, June 7 4:00 - 6:00pm | **Analog/Mixed-Signal/RF Design** | **Room: 31C**

18 ANALOG AND MIXED-SIGNAL DESIGN IN AN UNCERTAIN WORLD

Chair(s):
Trent McConaghy - *Solido Design Automation, Inc., Saskatoon, CA*

This session hosts recent innovations to combat the noise and variability issues faced in today's analog and mixed-signal circuits. The first two papers propose novel algorithms for simulating thermal, flicker, and random telegraph noise in the time domain. The next two papers focus on ways to ensure stability and performance of nanoscale analog circuits in the presence of process variation. The final two papers present ideas to improve the system reliability and new advances in reconfigurable analog designs.

18.1 MUSTARD: A Coupled, Stochastic-Deterministic, Discrete-Continuous Technique for Predicting the Impact of Random Telegraph Noise on SRAMs and DRAMs
Karthik V. Aadithya, Sriram Venugopalan, Jaijeet Roychowdhury - *Univ. of California, Berkeley, CA*
Alper Demir - *Koç Univ., Sariyer-Istanbul, Turkey*

18.2 Fast, Non-Monte-Carlo Transient Noise Analysis for High-Precision Analog/RF Circuits by Stochastic Orthogonal Polynomials
Fang Gong, Lei He - *Univ. of California, Los Angeles, CA*
Hao Yu - *Nanyang Technological Univ., Singapore, Singapore*

18.3 Automatic Stability Checking for Large, Linear Analog Integrated Circuits
Parijat Mukherjee, Peng Li - *Texas A&M Univ., College Station, TX*
G. Peter Fang, Rod Burt - *Texas Instruments, Inc., Dallas, TX*

18.4 Performance Bound Analysis of Analog Circuits Considering Process Variations
Zhigang Hao, Guoyong Shi - *Shanghai Jiao Tong Univ., Shanghai, China*
Sheldon X.-D. Tan, Ruijing Shen - *Univ. of California, Riverside, CA*

18.5 Rethinking Memory Redundancy: Optimal Bit Cell Repair for Maximum-Information Storage
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

18.6 Programmable Analog Device Array (PANDA): A Platform for Transistor-Level Analog Reconfigurability
Rui Zheng, Jounghyuk Suh, Cheng Xu, Bertan Bakkaloglu, **Yu Cao** - *Arizona State Univ., Tempe, AZ*
Nagib Hakim - *Intel Corp., Santa Clara, CA*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Wednesday, June 8 9:00 - 10:30am | General Interest | Room: 33ABC

19 PANEL: EDA RESEARCH: STALLED, DRIVING IN CIRCLES, OR RUNNING OUT OF GAS?

Chair(s):
William Joyner - *Semiconductor Research Corp., Research Triangle Park, NC*

Organizer(s):
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*

Speaker(s):
Robert Brayton - *Univ. of California, Berkeley, CA*
Philippe Magarshack - *STMicroelectronics, Crolles, France*
Charles Alpert - *IBM Corp., Austin, TX*
Rob A. Rutenbar - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Shankar Krishnamoorthy - *Mentor Graphics Corp., Fremont, CA*

Everyone seems frustrated with the inefficiencies in EDA Research. So who's to blame, and more importantly, who should fix it? One answer is that industry vendors need to take a more active role in supporting research. Or, should researchers focus more on real-world problems instead of generating papers? Come watch as these constituencies defend themselves, and in the end, you'll decide who is wasting gas!

Wednesday, June 8 9:00 - 10:30am | Verification and Test | Room: 29AB

20 SPECIAL SESSION: SCALING AND SECURITY: DOES MORE TRANSISTORS MEAN MORE SECURITY?

Chair(s):
Ken Mai - *Carnegie Mellon Univ., Pittsburgh, PA*

Organizer(s):
Soha Hassoun - *Tufts Univ., Medford, MA*

The unprecedented levels of integrated circuit performance, efficiency, and affordability enabled by process technology scaling has led to the pervasive deployment of microelectronic systems. Because these systems routinely store, manipulate, and transmit sensitive data, there is a strong and growing interest in building secure systems. This session discusses how process technology scaling has at once made the design and implementation of secure systems easier and harder. The talks present views of the implications of continued technology scaling for building secure systems and the state-of-the-art in semiconductor reverse engineering.

20.1 Complexity and the Challenges of Securing SOCs
Paul Kocher - *Cryptography Research, Inc., San Francisco, CA*

20.2 High Performance Energy-Efficient Encryption in the sub-45nm CMOS Era
Ram Krishnamurthy, Sanu Mathew, Farhana Sheikh - *Intel Corp., Hillsboro, OR*

20.3 The State-of-the-Art in Semiconductor Reverse Engineering
Randy Torrance, Dick James - *Chipworks Inc., Ottawa, ON, Canada*

Wednesday, June 8 9:00 - 10:30am | System-Level Design | Room: 29CD

21 NEED FOR SPEED: SYSTEM-LEVEL ANALYSIS AND DESIGN

Chair(s):
Luciano Lavagno - *Politecnico di Torino, Torino, Italy*

This session presents approaches for rapid simulation of multicore systems, design analysis, and performance optimization of maximum temperature and error-detection algorithms. The first two papers address fast parallel simulation for multicore systems by effective configuration of simulation platforms and their scheduling. The third paper addresses statistical performance analysis by correlating transaction models with RTL. The fourth paper effectively extracts design hierarchy modeled by SystemC. The last two papers focus on performance optimization under temperature constraints and for error detection mechanisms.

21.1 A High-Parallelism Distributed Scheduling Mechanism for Multicore Instruction-Set Simulation
Meng-Huan Wu, Peng-Chih Wang, Cheng-Yang Fu, Ren-Song Tsay - *National Tsing Hua Univ., Hsinchu, Taiwan*

21.2 Simulation Environment Configuration for Parallel Simulation of Multicore Embedded Systems
Dukyoung Yun, Jinwoo Kim, Soonhoi Ha - *Seoul National Univ., Seoul, Republic of Korea*
Sungchan Kim - *Chonbuk National Univ., Jeonju, Republic of Korea*

21.3 Transaction-Level Statistical Analysis for Efficient Microarchitectural Power and Performance Studies
Eman Copty, Gila Kamhi, Sasha Novakovsky - *Intel Corp., Haifa, Israel*

21.4 Extracting Behavior and Dynamically-Generated Hierarchy from SystemC Models
Harry Broeders, René van Leuken - *Delft Univ. of Technology, Delft, The Netherlands*

21.5 Throughput Maximization for Periodic Real-Time Systems Under the Maximal Temperature Constraint
Huang Huang, Gang Quan, Jeffrey Fan - *Florida International Univ., Miami, FL*
Meikang Qiu - *Univ. of Kentucky, Lexington, KY*

21.6 Performance Optimization of Error Detection Based on Speculative Reconfiguration
Adrian Alin Lifa, Petru Eles, Zebo Peng - *Linköping Univ., Linkoping, Sweden*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Wednesday, June 8 9:00 - 10:30am | **Embedded Systems and Software** | **Room: 30C**

22 TRENDS IN SYSTEM-LEVEL DESIGN SPACE EXPLORATION AND OPTIMIZATION

Chair(s):
Lothar Thiele - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*

This session consists of six papers covering different aspects of high-level system exploration and optimization. The first four papers address sustainability, extensibility, timing, and reliability issues in application domains such as automotive, multimedia, and mobile applications. The fifth paper proposes techniques for multi-objective design space exploration, and finally the sixth paper deals with system design using emerging memory technologies.

22.1 On the Quantification of Sustainability and Extensibility of FlexRay Schedules
Reinhard Schneider, Dip Goswami, Samarjit Chakraborty - *Technische Univ. München, Munich, Germany*
Unmesh D. Bordoloi, Petru Eles, Zebo Peng - *Linköping Univ., Linkoping, Sweden*

22.2 Generalized Reliability-Oriented Energy Management for Real-Time Embedded Applications
Baoxian Zhao, Hakan Aydin - *George Mason Univ., Fairfax, VA*
Dakai Zhu - *Univ. of Texas, San Antonio, TX*

22.3 Customer-Aware Task Allocation and Scheduling for Multi-Mode MPSOCs
Lin Huang, **Rong Ye**, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

22.4 Symbolic System Synthesis in the Presence of Stringent Real-Time Constraints
Felix Reimann, Michael Glaß, Christian Haubelt, Juergen Teich - *Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany*
Martin Lukasiewycz - *Technische Univ. München, Munich, Germany*

22.5 Supervised Design Space Exploration by Compositional Approximation of Pareto Sets
Hung-Yi Liu, Michele Petracca, Luca Carloni - *Columbia Univ., New York, NY*
Ilias Diakonikolas - *Univ. of California, Berkeley, CA*

22.6 Power-Aware Variable Partitioning for DSPs with Hybrid PRAM and DRAM Main Memory
Tiantian Liu, Yingchao Zhao, Chun Jason Xue, Minming Li - *City Univ. of Hong Kong, Kowloon, Hong Kong*

Wednesday, June 8 9:00 - 10:30am | **Verification and Test** | **Room: 31AB**

23 VALIDATION AND TEST: THE YIN AND YANG

Chair(s):
Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

Experience a true merger of validation and test in this session. The first paper applies efficient debug techniques to industrial designs. The second diagnoses the key causes of intermittent timing failures. The third provides enhanced ATPG efficiency for path-delay faults. Finally, the fourth improves timing failure diagnosis by handling multiple faults when their impact is complicated by clustering.

23.1 TAB-BackSpace: Unlimited-Length Trace Buffers with Zero Additional On-Chip Overhead
Flavio M. de Paula, Alan Hu - *Univ. of British Columbia, Vancouver, BC, Canada*
Amir Nahir, Ziv Nevo, Avigail Orni - *IBM Corp., Haifa, Israel*

23.2 Testability Driven Statistical Path Selection
Jaeyong Chung, Jacob A. Abraham - *Univ. of Texas, Austin, TX*
Jinjun Xiong, Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*

23.3 Diagnosing Scan Clock Delay Faults Through Statistical Timing Pruning
Mingjing Chen, **Alex Orailoglu** - *Univ. of California at San Diego, La Jolla, CA*

23.4 Diagnosis of Transition Fault Clusters
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

Wednesday, June 8 9:00 - 10:30am | **Low-Power Design** | **Room: 31C**

24 LEAKAGE POWER OPTIMIZATION

Chair(s):
David Garrett - *Broadcom Corp., Irvine, CA*

As the semiconductor industry continues its march down 32nm, leakage power continues to increase its dominance in the total power consumption. This session presents different exciting efforts to lower leakage power. The session starts with a paper that presents a leakage-aware redundancy for reliable subthreshold memories and continues with another that offers a 40nm subthreshold standard cell library, which takes inverse-narrow-width-effect into account. The session ends with two papers that propose line-edge roughness aware poly-layout optimization and post sign-off adjustments, respectively. The objective of both papers is to further reduce the leakage power.

24.1 Leakage-Aware Redundancy for Reliable Subthreshold Memories
Seokjoong Kim, Matthew Guthaus - *Univ. of California, Santa Cruz, CA*

24.2 A 40nm Inverse Narrow-Width, Effect-Aware Subthreshold Standard Cell Library
Jun Zhou - *Institute of Microelectronics, Singapore, Singapore*
Senthil Jayapal - *Intel Corp., Penang, Malaysia*
Ben Busze, Li Huang, **Jan Stuyt** - *Holst Centre, Eindhoven, The Netherlands*

24.3 Layout-Aware, Line-Edge Roughness Modeling and Poly-Optimization for Leakage Minimization
Yongchan Ban, Jae-Seok Yang - *Univ. of Texas, Austin, TX*

24.4 Post Sign-Off Leakage Power Optimization
Hamed Abrishami, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Jinan Lou - *Google, Inc., Mountain View, CA*
Jeff Qin, Juergen Froessl - *Synopsys, Inc., Mountain View, CA*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Wednesday, June 8 2:00 - 3:30pm | **System-Level Design** | **Room: 33ABC**

25 PANEL: SOFTWARE-HARDWARE VERIFICATION BATTLE: PROTOTYPING VS. EMULATION

Chair(s):
Bryon Moyer - *Techfocus Media, Inc., San Jose, CA*

Organizer(s):
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

Speaker(s):
Subhasish Mitra - *Stanford Univ., Stanford, CA*
Chris Tice - *Cadence Design Systems, Inc., San Jose, CA*
Avi Ziv - *IBM Corp., Haifa, Israel*
Joachim Kunkel - *Synopsys, Inc., Mountain View, CA*
Raj Yavatkar - *Intel Corp., Portland, OR*
Albert Camilleri - *Qualcomm, Inc., San Diego, CA*

In today's multiprocessor/multicore designs, it is becoming essential to verify software execution before committing to silicon. Some say prototyping is essential - but that could be by virtual prototype or by FPGA. Others say emulation is the way to go. Who is right? Experts from academia and the industry will wrestle with the question to determine the best way to success.

Wednesday, June 8 2:00 - 3:30pm | **DFM and the Manufacturing Interface** | **Room: 29AB**

26 SPECIAL SESSION: DESIGN AND TECHNOLOGY AT 14NM NODE: MYTHS AND REALITIES

Chair(s):
Geoffrey Yeap - *Qualcomm, Inc., San Diego, CA*

Organizer(s):
Ruchir Puri - *IBM Corp., Yorktown Hts., NY*
David Z. Pan - *Univ. of Texas, Austin, TX*

The semiconductor industry continues to battle the laws of physics on its march towards the next few technology nodes. As we move down this path, what are the design and technology challenges in store for our community? What are the kinds of research problems that we will need to solve? This session is intended to be an eye-opening experience that previews the pain that we may encounter in the 14nm era. The three invited talks will cover topics from lithography/ scaling to new transistor structures to circuit design challenges at 14nm and beyond.

26.1 Lithography at 14nm and Beyond: Choices and Challenges
Vivek Singh - *Intel Corp., Portland, OR*

26.2 New Sub-20nm Transistors - Why and How
Chenming Hu - *Univ. of California, Berkeley, CA*

26.3 Circuit Design Challenges at the 14nm Technology Node
James Warnock - *IBM Corp., Yorktown Hts., NY*

Wednesday, June 8 2:00 - 3:30pm | **Embedded Systems and Software** | **Room: 29CD**

27 PUNCTUAL SOFTWARE: IT'S ABOUT TIME

Chair(s):
Sami Yehia - *Thales Group, Palaiseau, France*

Timing - specifically the need to meet deadlines - distinguishes real-time software from the usual best-effort fare. The first paper in this session shows us how to meet deadlines while reducing a chip's operating temperature by throttling tasks with a greedy, leaky-bucket shaper. The second meets deadlines while running alongside best-effort Linux processes, which requires the whole Linux kernel to be preemptible. The next paper determines the execution time of synchronous software by considering which states and variable values are possible. The fourth shows how to quickly estimate target code speed by running it on a host processor, even when optimization makes the two binaries nearly incomparable.

27.1 Cool Shapers: Shaping Real-Time Tasks for Improved Thermal Guarantees
Lothar Thiele, Pratyush Kumar - *Eidgenössische Technische Hochschule Zürich, Zurich, Switzerland*

27.2 ChronOS Linux: A Best-Effort, Real-Time Multiprocessor Linux Kernel
Matthew Dellinger, Piyush Garyali, Binoy Ravindran - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

27.3 Efficient WCRT Analysis of Synchronous Programs Using Reachability
Matthew Kuo, Roopak Sinha, Partha S. Roop - *The Univ. of Auckland, Auckland, New Zealand*

27.4 Fast and Accurate Source-Level Simulation of Software Timing Considering Complex Code Optimizations
Stefan Stattelmann, Oliver Bringmann - *Forschungszentrum Informatik, Karlsruhe, Germany*
Wolfgang Rosenstiel - *Univ. Tübingen, Tuebingen, Germany*

TECHNICAL SESSIONS

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Wednesday, June 8 2:00 - 3:30pm | **Verification and Test** | **Room: 30C**

28 SYSTEM VERIFICATION: IS FORMAL THE NEW NORMAL?

Chair(s):
Naren Narasimhan - *Intel Corp., Hillsboro, OR*

Formal methods have shown great promise for the specification, development, and verification of software and hardware systems; this session comprises four new contributions. The first paper uses abstraction to enable formal verification of quality-of-service (QOS) properties on large scale NOCs. The second paper explores approaches to detect and prevent the possibility of global convergence failures in mixed-signal systems. The third paper analyzes a class of memory consistency models and establishes that small litmus tests suffice to distinguish different models. The final paper presents a new approach to simultaneously verify low-level software with the hardware on which it is running.

28.1 Abstraction-Based Performance Analysis of NOCs
Daniel E. Holcomb, Bryan A. Brady, Sanjit A. Seshia - *Univ. of California, Berkeley, CA*

28.2 Global Convergence Analysis of Mixed-Signal Systems
Sangho Youn, Jaeha Kim - *Seoul National Univ., Seoul, Republic of Korea*
Mark A. Horowitz - *Stanford Univ., Stanford, CA*

28.3 Litmus Tests for Comparing Memory Consistency Models: How Long Do They Need to Be?
Sela Mador-Haim, Rajeev Alur, Milo M.K. Martin - *Univ. of Pennsylvania, Philadelphia, PA*

28.4 Formal Hardware/Software Co-Verification by Interval Property Checking with Abstraction
Minh D. Nguyen, Markus Wedler, Dominik Stoffel, Wolfgang Kunz - *Technische Universität Kaiserslautern, Kaiserslantern, Germany*

Wednesday, June 8 2:00 - 3:30pm | **Physical Design** | **Room: 31AB**

29 CLOCKS AND CIRCUITS

Chair(s):
Bill Swartz - *Timberwolf Systems, Inc., Dallas, TX*

This session has four interesting papers on clocks and circuits. The first paper deals with resonant clock design for meshes, and the second paper proposes a new clock polarity buffer assignment algorithm with buffer sizing. The third paper proposes a novel approach to capacitance matching for analog circuits and the fourth paper presents new circuit structure to measure and characterize variations and SOI history effects.

29.1 Distributed Resonant Clock Grid Synthesis (ROCKS)
Xuchu Hu, Matthew Guthaus - *Univ. of California, Santa Cruz, CA*

29.2 WaveMin: A Fine-Grained Clock Buffer Polarity Assignment Combined with Buffer Sizing
Deokjin Joo, **Taewhan Kim** - *Seoul National Univ., Seoul, Republic of Korea*

29.3 Common-Centroid Capacitor Placement Considering Systematic and Random Mismatches in Analog Integrated Circuits
Cheng-Wu Lin, Jai-Ming Lin, Yen-Chih Chiu, Chun-Po Huang, Soon-Jyh Chang - *National Cheng Kung Univ., Tainan City, Taiwan*

29.4 Characterizing Within-Die and Die-to-Die Delay Variations Introduced by Process Variations and SOI History Effect
Charles Lamech, **Jim Aarestad**, Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*
Dhruva Acharyya - *Verigy Ltd., Santa Clara, CA*
Kanak Agarwal - *IBM Corp., Austin, TX*

Wednesday, June 8 2:00 - 3:30pm | **Interconnect and Reliability** | **Room: 31C**

30 MODEL REDUCTION AND ACCELERATED EXTRACTION

Chair(s):
Ibrahim Elfadel - *IBM Corp., Yorktown Hts., NY*

Papers in this session deal with improving efficiency and robustness of interconnect modeling and analysis. The techniques proposed are based on model reduction and accelerated capacitance extraction. The first two papers discuss stability preservation for nonlinear system models and accuracy improvements in passivity enforcement techniques for linear interconnect models. The following two papers discuss approaches for faster capacitance extraction by exploiting parallelism, either at the equation formulation and solution level, or through the use of GPU acceleration.

30.1 A Stabilized Discrete Empirical Interpolation Method for Model Reduction of Electrical, Thermal, and Microelectromechanical Systems
Amit Hochman, Jacob K. White - *Massachusetts Institute of Technology, Cambridge, MA*
Bradley N. Bond - *Sandia National Laboratories, Albuquerque, NM*

30.2 A Novel Framework for Passive Macromodeling
Zuochang Ye, Yang Li, Mingzhi Gao, Zhiping Yu - *Tsinghua Univ., Beijing, China*

30.3 A Highly Scalable Parallel Boundary Element Method for Capacitance Extraction
Yu-Chung Hsiao, Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*

30.4 Fast Multipole Method on GPU: Tackling 3-D Capacitance Extraction on Massively Parallel SIMD Platforms
Xueqian Zhao, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Wednesday, June 8 4:00 - 6:00pm | General Interest | Room: 33ABC

31 PANEL: THE BILLION DOLLAR QUESTION: HOW TO VERIFY BILLION-GATE DESIGNS

Chair(s):
Himanshu Bhatnagar - *Mindspeed Technologies, Inc., Newport Beach, CA*

Organizer(s):
Sandip Kundu - *Univ. of Massachusetts, Amherst, MA*

Speaker(s):
Dammy Olopade - *Intel Corp., Portland, OR*
Prakash Narain - *Real Intent, Inc., Sunnyvale, CA*
Kathryn Kranen - *Jasper Design Automation, Inc., Mountain View, CA*
David Hoenig - *NVIDIA Corp., Portland, OR*
Rowland Reed - *Qualcomm, Inc., Austin, TX*
Y.C. Wong - *Broadcom Corp., San Diego, CA*

Next-generation chips will contain literally billions of gates that need to be verified before committing to silicon. With billions of dollars at stake, the right solution is crucial for verifying designs susceptible to complex failures arising from corner-case confluences of timing and functionality. This panel will debate the merits of emerging solutions for such self-contained verification problems that threaten to subvert the nominal "simulation plus STA" verification flow.

Wednesday, June 8 4:00 - 6:00pm | Verification and Test | Room: 29AB

32 SPECIAL SESSION: PRE-SILICON VERIFICATION METHODS FOR POST-SILICON VALIDATION

Chair(s):
Andreas Veneris - *Univ. of Toronto, Toronto, ON, Canada*

Organizer(s):
Tim Cheng - *Univ. of California, Santa Barbara, CA*

Post-silicon functional and electrical validation consumes an increasing share of the overall product development time and cost. While new resources and infrastructure dedicated to post-silicon validation are necessary, it would be advantageous to leverage the enormous effort that goes into pre-silicon verification, including models, tools, tests, and metrics, for post-silicon purposes, This session explores the synergy between pre-silicon verification and post-silicon validation and reports some of recent industrial experiences. The papers in this session cover issues such as design for debug/validation, test development, improved functional testing, and design methodology issues.

32.1 Transaction Based Pre-to-Post Silicon Validation
Eli Singerman - *Intel Corp., Haifa, Israel*
Yael Abarbanel, Sean Baartmans - *Intel Corp., Hillsboro, OR*

32.2 Leveraging Pre-Silicon Verification Resources for the Post-Silicon Validation of the IBM POWER7 Processor
John Schumann, Charles Meissner - *IBM Corp., Austin, TX*
Allon Adir, Amir Nahir, Gil Shurek, Avi Ziv - *IBM Corp., Haifa, Israel*

32.3 A Method to Leverage Pre-Silicon Collateral and Analysis for Post-Silicon Testing and Validation
Gary Miller, Bandana Bhattarai - *Freescale Semiconductor, Inc., Austin, TX*
George Bakewell, Jay Dutt, Xi Chen, Yu-Chin Hsu - *SpringSoft, Inc., San Jose, CA*

Wednesday, June 8 4:00 - 6:00pm | Embedded Systems and Software | Room: 29CD

33 EMBEDDED SYSTEMS CASE STUDIES AND DESIGN METHODS

Chair(s):
Andreas Gerstlauer - *Univ. of Texas, Austin, TX*

This session presents compelling case studies based on sound design methodologies and application-specific design methods. The first paper deals with wireless embedded systems, focusing on multiple input/multiple output(MIMO) detection with low power. The second paper considers image construction with FPGAs, while the third investigates data driven biomedical monitoring algorithms. The fourth paper considers Ethernet audio/video bridging for automotive applications. The fifth paper explores ways to trade off quality for efficiency. The last paper presents a case study of throughput estimation for USB2.0.

33.1 Energy-Efficient MIMO Detection Using Unequal Error Protection for Embedded Joint Decoding System
Yoon Seok Yang, Pankaj Bhagawat, Gwan Choi - *Texas A&M Univ., College Station, TX*

33.2 An Algorithm-Architecture Codesign Framework for Gridding Reconstruction Using FPGAs
Srinidhi Kestur, Kevin M. Irick, Sungho Park, Ahmed Al Maashri, Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*
Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*

33.3 A Low-Energy Computation Platform for Data-Driven Biomedical Monitoring Algorithms
Mohammed Shoaib, Niraj K. Jha, Naveen Verma - *Princeton Univ., Princeton, NJ*

33.4 Accuracy of Ethernet AVB Time Synchronization Under Varying Temperature Conditions for Automotive Networks
Helge Zinner, Josef Nöbauer - *Continental AG, Regensburg, Germany*
Andreas Kern - *Daimler AG, Boeblingen, Germany*
Thilo Streichert, Juergen Teich - *Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany*

33.5 Dynamic Effort Scaling: Managing the Quality-Efficiency Tradeoff
Vinay Chippa, Anand Raghunathan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Srimat T. Chakradhar - *NEC Corp., Princeton, NJ*

33.6 Emulation-Based, High-Accuracy Throughput Estimation for High-Speed Connectivities: Case Study of USB2.0
Chulho Shin, Byungchul Hong, Daehyup Ko - *LG Electronics, Seoul, Republic of Korea*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Wednesday, June 8 4:00 - 6:00pm | **Synthesis and FPGA** | **Room: 30C**

34 LOGIC SYNTHESIS: OLD STORIES WITH NEW TWISTS

Chair(s):
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*

This session revisits several classic problems in synthesis and technology mapping. The presented papers open up new avenues for efficient solutions and raise important questions for further investigation. The first paper uncovers fine-grain parallelism in BDD reordering. The second one reduces overhead in clock gating functions for controllers. The third contribution proposes using distinct libraries for synthesis and placement in order to reduce active area and power. Finally, the last paper analyzes the stability of logic synthesis tools under behavior-preserving source code modifications.

34.1 Implicit Permutation Enumeration Networks and Binary Decision Diagrams Reordering
Stergios Stergiou - *Fujitsu Labs Ltd., Sunnyvale, CA*

34.2 Using SAT-Based Craig Interpolation to Enlarge Clock Gating Functions
Ting-Hao Lin, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

34.3 Power Reduction via Separate Synthesis and Physical Libraries
Mohammad M. Rahman, Ryan Afonso, Hiran Tennakoon, Carl Sechen - *Univ. of Texas at Dallas, Richardson, TX*

34.4 Are Logic Synthesis Tools Robust?
Alberto Puggelli, Tobias Welp, Andreas Kuehlmann, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Wednesday, June 8 4:00 - 6:00pm | **Physical Design** | **Room: 31AB**

35 3-D IC DESIGN

Chair(s):
Rakesh Patel - *GLOBALFOUNDRIES, Milpitas, CA*

This session brings together papers in the area of 3-D. The first paper analyzes layout effects in 3-D integrated microprocessor blocks. The second paper targets clock tree generation. The third paper presents an algorithm for through-silicon via (TSV) assignment. The fourth paper looks into non-uniform micro-channel assignment in 3-D chip cooling interconnections. The fifth paper targets TSV-aware placement. The final paper in the session looks into the problem of co-placement of cells and through-silicon vias (TSVs).

35.1 Layout Effects in Fine-Grain 3-D Integrated Regular Microprocessor Blocks
Vivek S. Nandakumar, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

35.2 Fault-Tolerant 3-D Clock Network
Chiao-Ling Lung, Shih-Hsiu Huang, Shih-Chieh Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yu-Shih Su - *Industrial Technology Research Institute, Hsinchu, Taiwan*
Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*

35.3 An Integrated Algorithm for 3-D IC TSV Assignment
Xiaodong Liu, Xuan Zeng - *Fudan Univ., Shanghai, China*
Yifan Zhang - *Synopsys, Inc., Shanghai, China*
Gary Yeap - Synopsys, Inc., Mountain View, CA

35.4 Non-Uniform Micro-Channel Design for Stacked 3-D ICs
Bing Shi, Ankur Srivastava, Peng Wang - *Univ. of Maryland, College Park, MD*

35.5 TSV-Aware Analytical Placement for 3-D IC Designs
Meng-Kai Hsu, **Yao-Wen Chang**, Valeriy Balabanov - *National Taiwan Univ., Taipei, Taiwan*

35.6 Thermal-Aware Cell and Through-Silicon-Via Co-Placement for 3-D ICs
Jason Cong, **Guojie Luo** - *Univ. of California, Los Angeles, CA*
Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*

Wednesday, June 8 4:00 - 6:00pm | **Interconnect and Reliability** | **Room: 31C**

36 ADVANCEMENT IN POWER INTEGRITY AND CIRCUIT RELIABILITY

Chair(s):
Marek Patyra - *Intel Corp., Hillsboro, OR*

Power integrity and circuit reliability are important issues for advanced technologies. The first three papers in this session discuss efficient verification and optimization methods for large-scale power delivery networks encountered in modern designs. The fourth paper discusses the single-event transient trends in future technologies. The fifth paper presents an elegant scrubbing method to improve the memory reliability in the presence of multiple cell upset. The last paper in the session presents the design of an in-field aging measurement and calibration circuit.

36.1 Efficient Incremental Analysis of On-Chip Power Grid via Sparse Approximation
Pei Sun, **Xin Li** - *Carnegie Mellon Univ., Pittsburgh, PA*
Ming-Yuan Ting - *Mentor Graphics Corp., Fremont, CA*

36.2 Power Grid Verification Using Node and Branch Dominance
Nahi Abdul Ghani, Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*

36.3 Power Grid Correction Using Sensitivity Analysis Under an RC Model
Pamela Al Haddad, Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*

36.4 Design Sensitivity of Single Event Transients in Scaled Logic Circuits
Jyothi Bhaskarr Velamala, Yu Cao - *Arizona State Univ., Tempe, AZ*
Robert LiVolsi, Myra Torres - *Impact Technologies, LLC, Rochester, NY*

36.5 Designing Ad-Hoc Scrubbing Sequences to Improve Memory Reliability Against Soft Errors
Pedro Reviriego, Juan Antonio Maestro - *Univ. Antonio de Nebrija, Madrid, Spain*
Sanghyeon Baeg - *Hanyang Univ., Kyung-Gi-Do, Republic of Korea*

36.6 In-Field Aging Measurement and Calibration for Power Performance Optimization
Shuo Wang, Mohammad Tehranipoor - *Univ. of Connecticut, Storrs, CT*
LeRoy Winemberg - *Freescale Semiconductor, Inc., Austin, TX*

TECHNICAL SESSIONS

BEST PAPER NOMINEES ARE DENOTED IN GREEN

Thursday, June 9 9:00 - 10:30am | **Embedded Systems and Software** | **Room: 33ABC**

37 PANEL: ESL HW/SW VERIFICATION: A REALITY CHECK

Chair(s):
Sharad Malik - *Princeton Univ., Princeton, NJ*

Organizer(s):
Daniel Große - *Univ. Bremen, Bremen, Germany*
Frank Schirrmeister - *Synopsys, Inc., Mountain View, CA*

Speaker(s):
Matthias Bauer - *Infineon Technologies AG, Neubiberg, Germany*
Viraphol Chaiyakul - *Qualcomm, Inc., San Diego, CA*
Alan Gatherer - *Huawei Technologies Co., Ltd., Dallas, TX*
Sandeep Shukla - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Daniel Kroening - *Oxford Univ., Oxford, United Kingdom*

ESL-based abstraction has become the preferred way to address the rising complexity of embedded system design. Academia and industry have invested huge amounts in creating integrated HW/SW design flows. But, will HW/SW verification become the show stopper? To answer that question, this panel will present several case studies that showcase the state of the art in HW/SW verification of embedded systems. In addition, several key open questions will be answered by the panelists.

Thursday, June 9 9:00 - 10:30am | **Bio Design Automation** | **Room: 29AB**

38 SPECIAL SESSION: CMOS SENSORS FOR BIOMEDICAL AND BIOLOGICAL APPLICATIONS

Chair(s):
Natasa Miskov-Zivnov - *Univ. of Pittsburgh, Pittsburgh, PA*

Organizer(s):
Iris Bahar - *Brown Univ., Providence, RI*

CMOS sensors, now common place in digital cameras, are now emerging as viable sensor technology for biological sensing, medical diagnostics and biomedical applications. This market for CMOS based biosensors is forecast to grow to a multi-billion dollar market in the coming decade. This new application domain places new challenges in sensor integration with CMOS technology, modeling and simulation technologies, and CAD tools and design methodologies. This session will highlight the potential and promise of biomolecular detection and biosensing, along with pressing challenges.

38.1 Single-Molecule Electronic Detection Using Nanoscale Field-Effect Devices
Sebastian Sorgenfrei, **Kenneth L. Shepard** - *Columbia Univ., New York, NY*

38.2 CMOS Compatible Nanowires for Biosensing
Eric Stern, David A. Routenberg, Aleksander Vacic, Nitin K. Rajan, Jason M. Criscione, Jason Park, Tarek M. Fahmy, **Mark Reed** - *Yale Univ., New Haven, CT*

38.3 Heterogeneous Integration of Carbon Nanotubes and Graphene on CMOS for Sensing Applications
Sameer R. Sonkusale - *Tufts Univ., Medford, MA*
Mehmet Dokmeci - *Northeastern Univ., Boston, MA*

Thursday, June 9 9:00 - 10:30am | **Emerging Technologies** | **Room: 29CD**

39 NOVEL ARCHITECTURES AND ALGORITHMS FOR MULTIPROCESSOR AND BIOLOGICAL APPLICATIONS

Chair(s):
Siddharth Garg - *Univ. of Waterloo, Waterloo, ON, Canada*

This session focuses on higher-level issues in emerging technologies. The first paper demonstrates that heterogeneous multiprocessor systems using a mix of CMOS and tunneling transistors is feasible. The second paper analyzes the behavior of optical interconnects in multiprocessor systems. The third paper presents a power-aware algorithm for addressing electrodes in microfluidic biochips. The last paper branches into a new area for DAC, and describes a new methodology to evaluate performance in biological pathways used for plant photosynthesis and microbial fuel cells.

39.1 An Energy-Efficient, Heterogeneous CMP Based on Hybrid TFET-CMOS Cores
Vinay Saripalli, Asit K. Mishra, Suman Datta, **Vijaykrishnan Narayanan** - *Pennsylvania State Univ., University Park, PA*

39.2 Device Modeling and System Simulation of Nanophotonic On-Chip Networks for Reliability, Power, and Performance
Zheng Li, Moustafa Mohamed, Xi Chen, Alan R. Mickelson, Li Shang - *Univ. of Colorado, Boulder, CO*

39.3 Progressive Network-Flow Based Power-Aware Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips
Tsung-Wei Huang, Hong-Yan Su, Tsung-Yi Ho - *National Cheng Kung Univ., Tainan City, Taiwan*

39.4 Design of Robust Metabolic Pathways
Renato Umeton - *Massachusetts Institute of Technology, Cambridge, MA*
Giovanni Stracquadanio - *Johns Hopkins Univ., Baltimore, MD*
Alessio Papini - *Univ. degli Studi di Firenze, Florence, Italy*
Anilkumar Sorathiya, Pietro Liò - *Univ. of Cambridge, Cambridge, United Kingdom*
Giuseppe Nicosia - *Univ. degli Studi di Catania, Catania, Italy*

TECHNICAL SESSIONS

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Thursday, June 9 9:00 - 10:30am | **Verification and Test** | **Room: 30C**

40 NEW METHODS AND METRICS IN TEST AND RELIABILITY

Chair(s):
Sagar Sabade - *Qualcomm, Inc., San Diego, CA*

This session begins with a study on reliability improvement for flash memories, and is followed by a discussion of improved quality metrics for CMOS imagers. Improved measurement and test access are also described with papers on jitter characterization and contactless testing.

40.1 Reliability Analysis and Improvement for Multi-Level, Non-Volatile Memories with Soft Information
Shih-Liang Chen, Bo-Ru Ke, Jian-Nan Chen, Chih-Tsun Huang - *National Tsing Hua Univ., Hsinchu, Taiwan*

40.2 Image-Quality-Aware Metrics for Performance Specification of ADC Array in 3-D CMOS Imagers
Hsiu-Ming Chang, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*

40.3 High-Effective Resolution Built-In Jitter Characterization with Quantization Noise Shaping
Leyi Yin, Yongtae Kim, Peng Li - *Texas A&M Univ., College Station, TX*

40.4 A Low-Cost Wireless Interface with No External Antenna and Crystal Oscillator for Cm-Range Contactless Testing
Chin-Fu Li, Chi-Ying Lee, Shu-Lin Chang, Tien-Yu Chang, Li-Ming Denq, Chun-Chuan Chi, Hsuan-Jung Hsu, Ming-Yi Chu, Chih-Tsun Huang, Shi-Yu Huang, Jing-Jia Liou, Po-Chiun Huang, Hsi-Pin Ma, Jenn-Chiou Bor, Cheng-Wen Wu - *National Tsing Hua Univ., Hsinchu, Taiwan*
Chen-Hsing Wang - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Chi-Hu Wang, Yung-Sheng Kuo, Ching-Cheng Tien - *Chung Hua Univ., Hsinchu, Taiwan*

Thursday, June 9 9:00 - 10:30am | **DFM and the Manufacturing Interface** | **Room: 31AB**

41 PANEL: 3-D: DEVILS, DETAILS, AND DEBATE

Chair(s):
Paul Franzon - *North Carolina State Univ., Raleigh, NC*

Organizer(s):
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

Speaker(s):
Raj Jammy - *SEMATECH, Austin, TX*
William Chen - *The Advanced Semiconductor Engineering Group, Sunnyvale, CA*
Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*
Matt Nowak - *Qualcomm, Inc., San Diego, CA*
Indavong Vongsavady - *STMicroelectronics, Crolles, France*

What a difference a year makes! It looks like 3-D has finally turned the corner with consumer products planned for the 32nm (or is it 28nm?) node. But devilish details - such as known-good die, standards, EDA tools, and flow signoff - could still become a showstopper. Panelists across the design ecosystem will shed light on which issues are still “devils” and those that are mere “details.”

Thursday, June 9 9:00 - 10:30am | **Emerging Technologies** | **Room: 31C**

42 CAD TECHNIQUES FOR ADVANCED PROCESS TECHNOLOGIES

Chair(s):
Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*

Advanced process technologies introduce significant design challenges that must be properly accounted for in a design flow. The first paper presents an efficient approach to cover all PVT corners in static timing analysis. The second paper investigates the crucial noise and timing implications introduced by through-silicon vias in advanced 3-D technologies. Paper number three proposes a 2-D layout decomposition methodology for spacer-type double-patterning lithography. The last paper presents a generic high-performance lithography-friendly detailed router for enhanced manufacturability.

42.1 A Fast Approach for Static Timing Analysis Covering All PVT Corners
Sari Onaissi, Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*
Feroze Taraporevala, Jinfeng Liu - *Synopsys, Inc., Mountain View, CA*

42.2 Full-Chip TSV-to-TSV Coupling Analysis and Optimization in 3-D IC
Chang Liu, Taigon Song, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*
Jonghyun Cho, Joohee Kim, Joungho Kim - *KAIST, Daejeon, Republic of Korea*

42.3 Flexible 2-D Layout Decomposition Framework for Spacer-Type Double-Patterning Lithography
Yongchan Ban, David Z. Pan - *Univ. of Texas, Austin, TX*
Kevin Lucas - *Synopsys, Inc., Austin, TX*

42.4 AENEID: A Generic Lithography-Friendly Detailed Router Based on Post-RET Data Learning and Hotspot Detection
Duo Ding, Jhih-Rong Gao, David Z. Pan, Kun Yuan - *Univ. of Texas, Austin, TX*

TECHNICAL SESSIONS

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Thursday, June 9 2:00 - 3:30pm | **DFM and the Manufacturing Interface** | **Room: 33ABC**

43 PANEL: DOUBLE TROUBLE OR DOUBLE YOUR FUN: DOUBLE-PATTERNING AND VARIABILITY

Chair(s):
Joe Sawicki - *Mentor Graphics Corp., Willsonville, OR*

Organizer(s):
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

The semiconductor industry faces extraordinary uncertainties at 20nm. The most pressing is what type of double-patterning to use and its impact on the entire flow. In addition, new device architectures and the explosion of variability and reliability effects must be managed. Panelists will discuss the critical risk factors at 20nm, the solutions that make the most dollars (and sense), and who should deliver those solutions.

Speaker(s):
Lars Liebmann - *IBM Corp., Hopewell Junction, NY*
Suk Lee - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Deepak Sherlekar - *Synopsys, Inc., Fremont, CA*
Rob Aitken - *ARM, Inc., San Jose, CA*
Diederik Verkest - *IMEC, Leuven, Belgium*
Jean-Pierre Geronimi - *STMicroelectronics, Crolles, France*

Thursday, June 9 2:00 - 3:30pm | **General Interest** | **Room: 29AB**

44 SPECIAL SESSION: REPURPOSING I.C. CAD COMPUTATIONAL TECHNIQUES FOR MOLECULAR AND CELL BIOLOGY

Chair(s):
Jaijeet Roychowdhury - *Univ. of California, Berkeley, CA*

Organizer(s):
L. Miguel Silveira - *INESC-ID/IST - TU Lisbon, Lisbon, Portugal*

Researchers in the biological sciences and designers of integrated circuits have two key attributes in common. First, their problems are so complicated that they must match the level of physical detail to the issue of interest; and second, circuit designers and biologists want tools that just work. It is therefore tempting, when faced with mathematically similar formulations in the two disciplines, to just plug an effective approach for the integrated circuit problem in to the biological problem. As the three examples in this session make clear, the two fields are rarely plug-compatible. The first paper uses techniques similar to those used in analyzing interconnect coupling capacitances to evaluate a recently developed non-local formulation for the electrostatic component of receptor-ligand binding affinity. The second paper addresses the numerical subtleties associated with adapting techniques commonly used to simulate circuit oscillators to the problem of computing biochemical oscillator parametric sensitivities.

The third paper of this session focuses on techniques for analyzing systems with variability, an issue of growing importance in integrated circuit design, but an absolutely central problem for biologists analyzing data from cell populations.

44.1 A Fast Solver for Nonlocal Electrostatics in Biomolecular Science and Engineering
Jaydeep P. Bardhan - *Rush Univ., Chicago, IL*
Andreas Hildebrandt - *Univ. des Saarland, Saarbrücken, Germany*

44.2 Biochemical Oscillator Sensitivity Analysis in the Presence of Conservation Constraints
Jared Toettcher - *Univ. of California, San Francisco, CA*
Anya R. Castillo, Bruce Tidor, Jacob White - *Massachusetts Institute of Technology, Cambridge, MA*

44.3 In Silico Synchronization of Cellular Populations Through Expression Data Deconvolution
Marisa C. Eisenberg, Joshua N. Ash, Dan Siegal-Gaskins - *Ohio State Univ., Columbus, OH*

Thursday, June 9 2:00 - 3:30pm | **Synthesis and FPGA** | **Room: 29CD**

45 COMPUTING FABRICS: CORES, LUTS, AND MOLECULES

Chair(s):
Philip Brisk - *Univ. of California, Riverside, CA*

This session presents results for current and future reconfigurable computing fabrics. The first paper shows that it is possible to perform FPGA technology mapping across multiple objectives without sacrificing significant quality in any one metric. The second paper describes a novel approach to high-level synthesis based on separating microarchitecture from behavioral description. A heterogeneous fabric where multiple cores share reconfigurable accelerators is proposed in the third paper. The final paper demonstrates the possibility of synchronous molecular computation through the synthesis of chemical clock signals.

45.1 MO-Pack: Many-Objective Clustering for FPGA CAD
Ali Akoglu, Senthilkumar Thoravi Rajavel - *Univ. of Arizona, Tucson, AZ*

45.2 Enforcing Architectural Contracts in High-Level Synthesis
Nikhil A. Patil, Ankit Bansal, Derek Chiou - *Univ. of Texas, Austin, TX*

45.3 Shared Reconfigurable Fabric for Multicore Customization
Liang Chen, Tulika Mitra - *National Univ. of Singapore, Singapore*

45.4 Synchronous Sequential Computation with Molecular Reactions
Hua Jiang, Marc Riedel, Keshab K. Parhi - *Univ. of Minnesota, Minneapolis, MN*

TECHNICAL SESSIONS

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Thursday, June 9 2:00 - 3:30pm | **Verification and Test** | **Room: 30C**

46 OUTSMARTING BUGS THROUGH INTELLIGENT SIMULATION

Chair(s):
Bernd Becker - *Universität Freiburg, Freiburg, Germany*

This session focuses on making simulation and emulation-based verification more intelligent. The first two papers present novel techniques for improving stimulus generation for simulation when incremental features are added to the design or when the design microarchitecture is modified. The third paper addresses partitioning a big design across a massively parallel, hardware-accelerated, emulation environment to minimize latency and communication overheads. The final paper presents techniques for efficient post-silicon debug of multi-threaded processors.

46.1 Facing the Challenge of New Design Features: An Effective Verification Approach
Wisam Kadry, Ronny Morad, Eli Almog, **Alex Goryachev** - IBM Corp., Haifa, Israel
Christopher A. Krygowski - *IBM Corp., Poughkeepsie, NY*

46.2 Learning Microarchitectural Behaviors to Improve Stimuli Generation Quality
Yoav Katz, Michal Rimon, Avi Ziv - *IBM Corp., Haifa, Israel*
Gal Shaked - *Technion - Israel Institute of Technology, Haifa, Israel*

46.3 Robust Partitioning for Hardware-Accelerated Functional Verification
Michael D. Moffitt, Mátyás A. Sustik, Paul G. Villarrubia - *IBM Corp., Austin, TX*

46.4 Threadmill: A Post-Silicon Exerciser for Multi-Threaded Processors
Allon Adir, Maxim Golubev, Shimon Landa, Amir Nahir, Gil Shurek, Vitali Sokhin, **Avi Ziv** - *IBM Corp., Haifa, Israel,*

Thursday, June 9 2:00 - 3:30pm | **Verification and Test** | **Room: 31AB**

47 PANEL: FROM IP TO SOC: WHAT IS THE BEST WAY TO VERIFY YOUR DESIGN?

Chair(s):
Laurent Ducousso - *STMicroelectronics, Grenoble, France*

Organizer(s):
Gabriele Saucier - *Design and Reuse, Grenoble, France*

Speaker(s):
Huy-Nam Nguyen - *Bull SAS, Paris, France*
Thomas Goust - *ST-Ericsson, Grenoble, France*
Lawrence Loh - *Jasper Design Automation, Inc., Mountain View, CA*
Gevorg Torjyan - *Synopsys, Inc., Mountain View, CA*

The challenges of verifying complex SOCs and IP blocks have stimulated the recent introduction of successive "new" verification technologies. This panel will discuss key IP verification approaches in the context of the full continuum of verification flows from IP to SOC. Specific technology areas will be highlighted including: verification at a higher (and mixed) level of abstraction, convergence/combination of dynamic verification techniques, and the role of formal technology and verification IP.

Thursday, June 9 2:00 - 3:30pm | **Emerging Technologies** | **Room: 31C**

48 NOVEL DESIGN AND ANALYSIS TOOLS FOR EMERGING DEVICES

Chair(s):
Ian O'Connor - *École Centrale de Lyon, Ecully, France*

The four papers in this session present novel designs and CAD tools to support promising emerging technologies. The first paper presents an integrated framework for variability-aware FinFET based caches. The second paper describes fine-grained power gating of functional units using nanoelectromechanical (NEMS) switches. Paper number three develops an automated synthesis tool using a binary decision diagram approach for reconfigurable circuits with single electron transistors. The final paper presents a novel design optimization flow of Universal Logic Modules using double-gate carbon nanotube transistors.

48.1 CACTI-FinFET: An Integrated Delay and Power Modeling Framework for FinFET-Based Caches Under Process Variations
Chun-Yi Lee, Niraj K. Jha - *Princeton Univ., Princeton, NJ*

48.2 A Case for NEMS-Based Functional-Unit Power Gating of Low-Power Embedded Microprocessors
Michael B. Henry, Meeta Srivastav, Leyla Nazhandali - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

48.3 Automated Mapping for Reconfigurable Single-Electron Transistor Arrays
Yung-Chih Chen, Chun-Yao Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Soumya Eachempati - *Intel Corp., Hillsboro, OR*
Suman Datta, Yuan Xie, Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*

48.4 Universal Logic Modules Based on Double-Gate Carbon Nanotube Transistors
Andrew Zukoski, **Xuebei Yang**, Kartik Mohanram - *Rice Univ., Houston, TX*

TECHNICAL SESSIONS

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Thursday, June 9 4:00 - 6:00pm | **General Interest** | **Room: 33ABC**

49 PANEL: PARALLEL OR PARALYZING: IS PARALLEL EDA WORTH THE TROUBLE?

Chair(s):
Giovanni De Micheli - *EPFL-LEG, Lausanne, Switzerland*

Organizer(s):
Wolfgang Rosenstiel - *Univ. Tübingen, Tuebingen, Germany*

Speaker(s):
Patrick Madden - *SUNY Binghamton, Binghamton, NY*
Dipanjan Gope - *Physware, Inc., Mountain View, CA*
Guy Maor - *Extreme DA Corp., Santa Clara, CA*
Peng Li - *Texas A&M Univ., College Station, TX*
Bor-Yiing Su - *Univ. of California, Berkeley, CA*
Andrei Vladimirescu - *Univ. of California, Berkeley, CA*

The advent of ubiquitous multicore processors has made parallelization of EDA software an attractive proposition. The reality has been anything but that. As it turns out, it is REALLY hard! These panelists explain what it takes to parallelize real applications and where parallelization is a dead end.

Thursday, June 9 4:00 - 6:00pm | **Embedded Systems and Software** | **Room: 29AB**

50 SPECIAL SESSION: VIRTUALIZATION IN EMBEDDED SYSTEMS

Chair(s):
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*

Organizer(s):
Christoph Kirsch - *Univ. Salzburg, Salzburg, Austria*

Longer battery life? Simpler storage administration? More effective embedded systems? Virtualization is a "megatrend" and promises to solve all these problems and more. What are the roadblocks ahead of this rejuvenated 50-year old technology? This session will present challenges and solutions in virtualization at four levels of abstraction: software-process-level virtualization on ARM, language-level VM-based virtualization for Java on embedded systems, OS-level microkernel-based virtualization of embedded systems, and heterogeneous hardware-level virtualization of CPUs, GPUs, and FPGAs (dubbed "liquid metal").

50.1 Virtualization of Heterogeneous Machines
Joshua Auerbach, **David F. Bacon**, Perry Cheng, Rodric Rabbah, Sunul Shukla - *IBM Corp., Hawthorne, NY*

50.2 Process-Level Virtualization for Runtime Adaptation of Embedded Software
Kim Hazelwood - *Univ. of Virginia, Charlottesville, VA*

50.3 Virtualizing Embedded Systems - Why Bother?
Gernot Heiser - *NICTA and Univ. of New South Wales, Sydney, Australia*

50.4 Virtualizing Real-Time Embedded Systems with Java
Jan Vitek - *Purdue Univ., West Lafayette, IN*

Thursday, June 9 4:00 - 6:00pm | **Interconnect and Reliability** | **Room: 29CD**

51 TOWARDS RELIABLE AND ENERGY-MINIMAL NOC DESIGN

Chair(s):
Federico Angiolini - *iNoCs, Lausanne, Switzerland*

This session discusses methods to provide reliability, energy-efficient recovery, and performance-power optimizations in the latest NOC designs. The first two papers of the session present schemes to provide distributed recovery and fault-tolerant NOC architectures. Papers three and four propose variation-aware routing and system-level fault modeling approaches. The session concludes with two papers which address power and performance optimization schemes for nano-scale NOCs.

51.1 DRAIN: Distributed Recovery Architecture for Inaccessible Nodes in Multicore Chips
Andrew DeOrio, Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*
Konstantinos Aisopos - *Princeton Univ., Princeton, NJ*
Li-Shiuan Peh - *Massachusetts Institute of Technology, Cambridge, MA*

51.2 A Fault-Tolerant NOC Scheme Using Bidirectional Channel
Wen-Chung Tsai, Deng-Yuan Zheng, **Sao-Jie Chen** - *National Taiwan Univ., Taipei, Taiwan*
Yu-Hen Hu - *Univ. of Wisconsin, Madison, WI*

51.3 Process Variation-Aware Routing in NOC-Based Multicores
Akbar Sharifi, Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*

51.4 Enabling System-Level Modeling of Variation-Induced Faults in Networks-on-Chips
Konstantinos Aisopos - *Princeton Univ., Princeton, NJ*
Chia-Hsin Owen Chen, Li-Shiuan Peh - *Massachusetts Institute of Technology, Cambridge, MA*

51.5 FlexiBuffer: Reducing Leakage Power in On-Chip Network Routers
Gwangsun Kim, John Kim - *KAIST, Daejeon, Republic of Korea*
Sungjoo Yoo - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

51.6 Capacity Optimized NOC for Multi-Mode SOC
Isask'har Walter, **Erez Kantor**, Israel Cidon, Shay Kutten - *Technion - Israel Institute of Technology, Haifa, Israel*

TECHNICAL SESSIONS

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Thursday, June 9 4:00 - 6:00pm | **Embedded Systems and Software** | **Room: 30C**

52 DON'T FORGET MEMORY: PERFORMANCE AND RELIABILITY ISSUES IN CACHE, SCRATCHPAD, AND PRAM

Chair(s):
Jason Xue - *City Univ. of Hong Kong, Kowloon, Hong Kong*

This session explores performance, energy, and reliability issues in the memory hierarchy. The first two papers propose novel dynamic cache-partitioning techniques for multi-cores to improve performance and energy consumption. The third paper presents a reuse-aware prefetching algorithm for scratchpad memory. The fourth paper enables allocation of portions of SRAM cache as private buffers for accelerators in SOC. The final two papers deal with enhancing wear leveling in PRAM to include endurance variations and to minimize accesses to faulty words in SRAM cache, respectively.

52.1 Dynamic Cache Reconfiguration and Partitioning for Energy Optimization in Real-Time Multicore Systems
Weixun Wang, Prabhat Mishra, Sanjay Ranka - *Univ. of Florida, Gainesville, FL*

52.2 A Helper Thread Based Dynamic Cache Partitioning Scheme for Multithreaded Applications
Mahmut Kandemir, **Emre Kultursay** - *Pennsylvania State Univ., University Park, PA*
Taylan Yemliha - *Syracuse Univ., Syracuse, NY*

52.3 A Reuse-Aware Prefetching Scheme for Scratchpad Memory
Jason Cong, **Hui Huang**, Chunyue Liu, Yi Zou - *Univ. of California, Los Angeles, CA*

52.4 Buffer-Integrated-Cache: A Cost-Effective SRAM Architecture for Handheld and Embedded Platforms
Carlos A. Flores Fajardo, German Fabila Garcia - *Intel Corp., Guadalajara, Mexico*
Zhen Fang, Ravi R. Iyer, Li Zhao - *Intel Corp., Hillsboro, OR*
Seung Eun Lee - *Seoul National Univ., Seoul, Republic of Korea*

52.5 Wear Rate Leveling: Lifetime Enhancement of PRAM with Endurance Variation
Jianbo Dong, Lei Zhang, Yinhe Han, Ying Wang, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

52.6 Matching Cache Access Behavior and Bit Error Pattern for High Performance Low Vcc L1 Cache
Young Geun Choi, Sungjoo Yoo, Sunggu Lee - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*
Jung Ho Ahn - *Seoul National Univ., Seoul, Republic of Korea*

Thursday, June 9 4:00 - 6:00pm | **Low-Power Design** | **Room: 31AB**

53 ULTRA-LOW VOLTAGE AND POWER-AWARE DESIGN

Chair(s):
Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

This session presents important power-aware design contributions. The first two papers introduce novel power design, estimation, and optimization techniques for ultra-low voltage integrated circuits. The next two papers cover important problems in power delivery network analysis and design strategies. A new path-delay shaping method for error-resilient circuits is discussed in the fifth paper. This session concludes with a paper on power gating for current-mode logic.

53.1 A Closed-Form Expression for Estimating Minimum Operating Voltage (VDDmin) of CMOS Logic Gates
Hiroshi Fuketa, Satoshi Iida, Tadashi Yasufuku, Makoto Takamiya, Takayasu Sakurai - *The Univ. of Tokyo, Tokyo, Japan*
Masahiro Nomura, Hirofumi Shinohara - *STARC, Tokyo, Japan*

53.2 Pipeline Strategy for Improving Optimal Energy Efficiency in Ultra-Low Voltage Design
Mingoo Seok, **Dongsuk Jeon**, David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*

53.3 Fast Algorithms for IR Voltage Drop Analysis Exploiting Locality
Selçuk Köse, Eby G. Friedman - *Univ. of Rochester, Rochester, NY*

53.4 Decoupling for Power Gating: Sources of Power Noise and Design Strategies
Tong Xu, Peng Li, Boyuan Yan - *Texas A&M Univ., College Station, TX*

53.5 Error-Resilient Low-Power DSP via Path-Delay Shaping
Paul N. Whatmough, Shidhartha Das, David Bull - *ARM, Ltd., Cambridge, United Kingdom*
Izzat Darwazeh - *Univ. College London, London, United Kingdom*

53.6 Power-Gated MOS Current Mode Logic (PG-MCML): A Power-Aware DPA-Resistant Standard Cell Library
Alessandro Cevrero, Michael Schwander, Stéphane Badel, Paolo Ienne, Yusuf Leblebici - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*
Francesco Regazzoni - *Univ. Catholiqué de Louvain, Baaschtnech, Belgium*

Thursday, June 9 4:00 - 6:00pm | **Embedded Systems and Software** | **Room: 31C**

54 SPECIALIZED PROCESSING SYSTEMS FOR EMBEDDED COMPUTING

Chair(s):
Andreas Gerstlauer - *Univ. of Texas, Austin, TX*

Specializing processor systems for particular application domains can yield tremendous improvements in performance, power, and other metrics. The first paper describes a multicore system with novel hardware for fast feature extraction during vision processing. The second paper uses specialized memory to reduce energy during video coding. A pipelined multicore architecture adaptable to workload and illustrated on a video encoder is described in paper three. Paper four extends a Java processor with hardware to efficiently handle reactive and other embedded systems language constructs. Using ubiquitous CPU/GPU platforms for fast network routing is demonstrated in paper five. The final paper describes an open-source system simulator for multicore x86 systems.

54.1 EFFEX: An Embedded Processor for Computer Vision-Based Feature Extraction
Jason Clemons, Andrew Jones, Robert Perricone, Silvio Savarese, Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

54.2 Run-Time Adaptive Energy-Aware Motion and Disparity Estimation in Multiview Video Coding
Bruno Zatt - *Univ. Federal do Rio Grande do Sul and Karlsruher Institut für Technologie, Karlsruhe, Germany*
Muhammad Shafique, Jörg Henkel - *Karlsruher Institut für Technologie, Karlsruhe, Germany*
Felipe Sampaio, Luciano Agostini - *Univ. Federal de Pelotas, Pelotas, Brazil*
Sergio Bampi - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

54.3 Low-Power Adaptive Pipelined MPSOCs for Multimedia: An H.264 Video Encoder Case Study
Haris Javaid, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*
Muhammad Shafique, Jörg Henkel - *Karlsruher Institut für Technologie, Karlsruhe, Germany*

54.4 RJOP - A Customized Java Processor for Reactive Embedded Systems
Muhammad Nadeem, **Morteza Biglari-Abhari**, Zoran Salcic - *The Univ. of Auckland, Auckland, New Zealand*

54.5 Hermes: An Integrated CPU/GPU Microarchitecture for IP Routing
Yuhao Zhu - *Univ. of Texas, Austin, TX*
Yangdong Deng, Yubei Chen - *Tsinghua Univ., Beijing, China*

54.6 MARSSx86: A Full System Simulator for Mulitcore x86 CPUs
Avadh Patel, Furat Afram, Shunfei Chen, Kanad Ghose - *SUNY Binghamton, Binghamton, NY*

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Tuesday, June 7 10:30am - 12:00pm | System-Level Design | Room: 30DE

1U SYSTEM-LEVEL DESIGN, MODELING, AND VALIDATION

Chair(s):
Benjamin Carrion Schafer - *NEC Corp., Kawasaki, Japan*

System-level design requires new methodologies for dealing with the large scale and complexity encountered in typical designs. This session considers techniques for design, analysis, and validation at the system level. Presentations will cover processor power modeling and analysis by individual instructions, building an emulation-based testbench, converting existing RTL to the IP-XACT open standard, and an IP-XACT packaging and assembly flow.

1U.1 PowerMixer-IP: Instruction-Level Power Modeling for Processors

Shan-Chien Fang - *TinnoTek Inc., Hsinchu, Taiwan*
Chen-Wei Hsu, **Chia-Chien Weng**, Shi-Yu Huang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Chen-Wei Hsu - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Wen-Tsan Hsieh, Jen-Chieh Yeh - *Industrial Technology Research Institute, Hsinchu, Taiwan*

1U.2 Using Transactor-Based Emulation with Real-Time Traffic Generator in Networking SOC

James Yu - *Nokia Siemens Networks, Mountain View, CA*

1U.3 A Quick and Efficient Way to Migrate to an Effective IP-XACT Based Integration Methodology

Saurin Patel, Mukesh Chopra, Sparsh Arun - *STMicroelectronics, Greater Noida, India*

1U.4 Enriched IPXACT Based Packaging and Assembly Methodology with ConfigurableIP, CheckXml, VirtualIP, and ExportPattern Approach

Saurin Patel, Mukesh Chopra, Bhawna Chopra, Sparsh Arun, Nikhil Jaggia - *STMicroelectronics, Greater Noida, India*

Tuesday, June 7 1:00 - 2:00pm | User Track | Room: OUTSIDE ROOM 33ABC

2U POSTER SESSION

Embedded Systems and Software / Front-End Silicon Design Topics

2U.1 A Tool for the Automated Generation of Streaming SOCs

David Zaretsky, Gaurav Mittal, Lei Gao, Prith Banerjee - *Binachip, Inc., Chicago, IL*

2U.2 An Automated Methodology for Creating Complex SOC Derivatives

Midhun Chandran, Manoj Parameswaran, Rajon Ravimony - *Wipro Technologies, Kochi, India*
Hari Pendurty - *Texas Instruments, Inc., Stafford, TX*

2U.3 Case Study on Automatic Generation of Device Drivers Using the DDGEN Methodology

Manjunath Bettegowda, Venkataraghavan PK, Lokesh Kabra - *Synopsys, Inc., Bangalore, India*
Rayagond Kokatanur, Sandeep Pendharkar - *Vayavya Labs Pvt., Ltd., Bangalore, India*

2U.4 Embedded Software Driven System Validation and Test Using Virtual Prototypes

Achim Nohl, Victor Reyes, Filip Thoen, Frank Schirrmeister - *Synopsys, Inc., Mountain View, CA*

2U.5 Server Techniques Meet Embedded ARM Verification Challenges

Karen Holtz, Elena Tsanko - *IBM Corp., Haifa, Israel*
Duaa Jahshan - *Marvell Semiconductor, Inc., Yokneam, Israel*

2U.6 The Building Blocks for Design Productivity

Tali Dolev, Nir Antebi, Alex Barapp, Noam Ambar - *Intel Corp., Haifa, Israel*

2U.7 A Case Study on Adopting a Flexible FPGA Verification Methodology

Yi-Fan Chen, Tso-Yi Fan, Shih-Hsueh Chang, Jen-Chieh Yeh - *Industrial Technology Research Institute, Hsinchu, Taiwan*
Nan-Ting Yeh - *SpringSoft, Inc., Hsinchu, Taiwan*

2U.8 A Flow to Generate Optimal Diagnostic Test Pattern Set

Arjun Gill, Srinivas K. Vooka, Prashant M. Kulkarni - *Texas Instruments, Inc., Bengaluru, India*

2U.9 Accelerating Mixed-Signal Design Verification with Automated Behavioral Model Generation

Elena Raciti, Pierluigi Daglio - *STMicroelectronics, Agrate Brianza, Italy*
Pietro Vergine - *Leading Edge Snc., Bergamo, Italy*

2U.10 Achieving Scalable Verification of an AHB Interconnect with Variable Width Shims Using OVM-Based Multi-View Verification Components

Ashish Kumar - *Mentor Graphics Corp., Bangalore, India*
Vijayabhaskar Sankaranarayanan - *Cypress Semiconductor Corp., Bangalore, India*

2U.11 Achieving Vertical Reusability in OVM for Scalable Verification Environment

Parag Goel - *AppliedMicro, Inc., Pune, India*
Ashish Kumar - *Mentor Graphics Corp., Bangalore, India*

2U.12 Automated Approach to Register Design and Verification of Complex SOC

Ballori Banerjee, Silpa Naidu, **Subashini Rajan** - *LSI Corp., Bangalore, India*

2U.13 Automated Management of Verification Waivers

Gero Dittmann - *IBM Corp., Boeblingen, Germany*

2U.14 Automatic Generation of Interface Protocol Converter Using Model Checking Tool

Young-Il Kim - *Silicon Image, Inc., Sunnyvale, CA*

2U.15 Automation in Micro-Architectural Work-Flow for Efficient System-Level Protocol Verification

Muhammad K. Mhameed - *Intel Corp., Umm El Fahm, Israel*

2U.16 Efficient Failure Probability Analysis of SRAM Cells

Tzu-Teng Lin, Steve Tsai, Willis Shih, Nan-Chiun Lien, Yu-Tein Tsai - *Faraday Technology Corp., Hsinchu, Taiwan*

2U.17 Focused SOC Verification Through Functional Qualification

Rajesh Kapilashrami, Björn Fjellborg - *Ericsson, Stockholm, Sweden*

2U.18 Formal Verification Excels as Design Tool in Pre- and Post-Silicon Validation

Kaveri Pant - *Broadcom Corp., San Jose, CA*

2U.19 Framework Bridging the Gaps in Low-Power Verification

Neha Bajaj, Kaustav Guha, Ankush Bagotra - *Synopsys, Inc., Bangalore, India*

2U.20 How Formal Methodology Shrank the Verification Schedule of a Complex Statistics Block by 6x

Chirag Agarwal, Sandesh Borgaonkar - *Oski Technology, Inc., Mountain View, CA*
Rajesh Kothari - *Cisco Systems, Inc., San Jose, CA*
Darrow Chu - *Cadence Design Systems, Inc., San Jose, CA*

2U.21 Need for Both Verilog and System Verilog

Steven Meyer - *Pragmatic C Software Corp., Minneapolis, MN*

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Tuesday, June 7 2:00 - 3:30pm | **Embedded Systems and Software** | **Room: 30DE**

3U CASE STUDIES IN SYSTEMS AND SOFTWARE

Chair(s):

Miroslav Velev - *Aries Design Automation, LLC, Chicago, IL*

Many systems, especially embedded systems, are complex combinations of hardware and software. This session contains four case studies: using SystemC to model Serial Rapid I/O interconnect topologies, using SystemC and TLM 2.0 to model a satellite control computer, an automatic way to map applications into the memory hierarchy of an MPSOC, and using FPGAs to validate IP blocks.

3U.1 virSRIO: A Simple Simulation Methodology to Virtualize SRIO Model IO and Realize Complex Interconnect Topology
Nizamudheen Ahmed, Manivannan E - *Texas Instruments, Inc., Bangalore, India*

3U.2 Using a TLM Virtual Platform for System Performance Analysis and Software Optimization
Michael Bradley, Jon McDonald - *Mentor Graphics Corp., Jacksonville, FL*
Matthew Muskovac, Clifford Kimmery - *Honeywell International Inc., Clearwater, FL*

3U.3 MNEMEE – An Automated Toolflow for Parallelization and Memory Management in MPSOC Platforms
Arindam Mallik - *IMEC, Leuven, Belgium*

3U.4 FPGA Embedded Systems for Validation of Intellecutal Property Blocks
VJ Sananda - *Advanced Micro Devices, Inc., Austin, TX*

Tuesday, June 7 4:00 - 6:00pm | **Physical Design** | **Room: 30DE**

4U TIMING IS EVERYTHING

Chair(s):

Srinivas Nori - *GLOBALFOUNDRIES, Sunnyvale, CA*

Timing convergence continues to be one of the top priorities in IC design. In this session, presenters from major design houses will overview their solutions for timing closure. Presentations discuss SSTA methods for timing and robustness, a method for validating AOCV-based timing, timing models for clock domain crossing, and a specialized automatic solution for hold fixing in MCMM.

4U.1 SSTA Driven Design Robustness Analysis
Ajoy Mandal, Arvind N V, Frank Cano, Anthony Hill, Venkatraman Ramakrishnan, Satyendra Datla, Nicolas Verkinderen - *Texas Instruments, Inc., Nice, France*

4U.2 Practical Timing Sign-Off Method Using Statistical STA in 45nm Mobile Products
Kim Byung-Su, **Bong Hyun Lee**, Heo Sunik, Hungbok Choi - *Samsung, Yongin, Republic of Korea*

4U.3 Experimental Methodology for Validating Timing Closure with Advanced On-Chip Variation (AOCV)
Ramnath Venkatraman, Alex Tetelbaum, Ruggero Castagnetti - *LSI Corp., Milpitas, CA*

4U.4 Blackbox Timing Model Generation for Latch-Based Microprocessor Macros
Yaping Zhan, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

4U.5 Asynchronous Clock Domain Crossings Aware Physical Implementation of ASICs
Ramesh Rajagopalan, Namit Gupta - *Cisco Systems, Inc., San Jose, CA*
Ajay Bhandari - *Cisco Systems, Inc., San Jose, CA*

4U.6 Automated and Scalable Multi-Mode, Multi-Corner Hold Fixing
Sudhir Jain - *Freescale Semiconductor, Inc., Noida, India*

Wednesday, June 8 9:00 - 10:30am | **Physical Design** | **Room: 30DE**

5U ULTRA-DEEP, SUB-MICRON PHYSICAL OPTIMIZATION

Chair(s):

Raj Varada - *Intel Corp., Santa Clara, CA*

Physical design optimization constitutes a significant part of the design process, particularly in the face of increasing rule complexity in advanced semiconductor processes. The papers in this session discuss techniques for physical optimization, including pattern-based physical verification for yield improvement, an OpenAccess chip integration platform, mixed-signal verification, and variability characterization for memory blocks in 32nm process technology.

5U.1 Pattern-Based Physical Verification in the Design Flow
Cristopher Magalang, Valerio Perez, **Edward Teoh**, Rainer Mann, Vito Dai, Sky Yeo, Colin Hui - *GLOBALFOUNDRIES, Singapore*

5U.2 A Post-Layout Mixed-Signal Design Verification Flow with Silicon-Faithful Behavioral Model Extraction
Tatsuya Shirakawa, Saburo Hojo, Kunihiko Tsuboi - *STARC, Yokohama-shi, Japan*

5U.3 Statistical Characterization of a High-K Metal Gate 32nm ARM926 Core Under Process Variability Impact
Miguel Miranda, Paul Zuber, Petr Dobrovolny - *IMEC, Leuven, Belgium*
Selma Laabidi, Virgile Javerliac, Yves Laplanche - *ARM, Ltd., Grenoble, France*

5U.4 eFinale – Integration Platform for High Performance Processor Design
Rama Gopal Gandham, Jose Neves, Adam Matheny, Edward Hughes, Robert Averill III, Walter Nop - *IBM Corp., Poughkeepsie, NY*

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Wednesday, June 8 1:00 - 2:00pm | User Track | Room: OUTSIDE ROOM 33ABC

6U POSTER SESSION

Front-End and Back-End Silicon Design Topics

6U.1 Paging for Multicore: How We Increased Our Throughput on High-Memory Verification Jobs on Compute Farms
Shankar Hemmady, Amit Sharma, Shekhar Basavanna - *Synopsys, Inc., Bangalore, India*
Srinivasan Venkataramanan - *CVC Pvt., Ltd., Bangalore, India*

6U.2 PAVE: A Framework for Power Intent Verification
Diganchal Chakraborty - *Synopsys, Inc., Bangalore, India*

6U.3 Proving Constraints in Template-Based Circuit Designs
Arun Chandra - *Advanced Micro Devices, Inc., Santa Clara, CA*

6U.4 Reuse Experience of eVCs in SystemVerilog Verification Environment
Youngmin Kim, Namdo Kim, Byeong Min, **Jay B. Kim** - *Samsung, Yongin-City, Republic of Korea*

6U.5 RTL Insertion and Verification of an IBM MBIST Architecture for Hierarchical Design of a 32nm ASIC
Michael R. Ouellette, **Michael A. Ziegerhofer** - *IBM Corp., Essex Junction, VT*

6U.6 SOC Debugging on FPGA-Based HW Assisted Verification Platforms
Jim Wolfe - *Zoran Corp., Burlington, MA*
Donald Cramb - *EVE-USA, Inc., San Jose, CA*

6U.7 Template-Based Systematic Constraint Extraction for Faster CDC Verification Closure
Ashish Hari, Yogesh Badaya - *Mentor Graphics Corp., Noida, India*

6U.8 Timing-Driven CDC Verification Methodology -- Efficient Flow to Eliminate the Disconnect Between the Front-End and the Back-End
Himanshu Bhatnagar - *VLSI Technology, Inc., Newport Beach, CA*

6U.9 A Lean Approach Towards Efficient Block Design
Sumit Goswami, Vadivel Ramalingam, Amit Dounde - *Intel Corp., Bangalore, India*

6U.10 A Novel Cost-Effective Approach for Accurate Early Power Network Synthesis for Power-Gated SOCs
Anusha Gudla, Raju Rakha, Shrikrishna Mehetre - *Open-Silicon, Inc., Bangalore, India*

6U.11 A Power Distribution Network Modeling and Analysis Flow in 3-D ICs
Xiang Hu - *Univ. of California at San Diego, La Jolla, CA*

6U.12 Achieving High Scan Compression with a Low Pin-Count Test
Debo Sekoni - *AltaSens, Inc., Westlake Village, CA*

6U.13 Application of Extreme Computing Solutions for Significant Design Cycle Time Reduction
Andrew Spix - *Intel Corp., Santa Clara, CA*

6U.14 Application of TSV in ASIC Design
Prasad Subramaniam - *eSilicon Corp., Murray Hill, NJ*

6U.15 Automated Flow for Generating CMOS Custom Memory Bit Map Information
Nadeem Eleyan, Greg Seok, Hong Kim, Tung Pham, Rich McAuliffe - *Qualcomm, Inc., San Diego, CA*

6U.16 Automating RF Noise Reduction in a Mobile Application
Tobias Bjerregaard, Isac Jensen, Kristian Borum - *Teklatech A/S, Copenhagen K, Denmark*
Ulrich Roettcher, Hasan Ayguenes, Dirk-Steffen Bock, Hummaduddin Mohammed - *Toshiba Corp., Dusseldorf, Germany*

6U.17 Congestion Reduction by Iterated Spreading Placement Optimization
Gi-Joon Nam, Li Zhuo, Natarajan Viswanathan, Charles Alpert - *IBM Corp., Austin, TX*

6.18 Consistency Checking Solution for LEF and GDSII Views
Zia Ahmed - *GLOBALFOUNDRIES, Singapore*

6U.19 Conversion and Optimization Flow for Analog IP Porting
Udo Sobe, Achim Graupner, Enno Böhme - *ZMDI, Dresden, Germany*
Michael Pronath - *Mun EDA GmbH, Munich, Germany*

6U.20 Defect Pattern Library Construction for the Lithography Hotspot Pattern Search Based on a Two-Level, 2-D Pattern Matching
Shunji Saika - *Panasonic Corp., Kyoto, Japan*

Wednesday, June 8 2:00 - 3:30pm | Low-Power Design | Room: 30DE

7U NEW FRONTIERS IN POWER

Chair(s):
Miguel Miranda - *IMEC, Leuven, Belgium*

Power/performance trade-offs continue to define the next generation of silicon designs. Power is a top focus for applications that range from always-on servers to mobile computing devices, and power optimization is pervasive throughout the design process. The presentations in this session discuss power gate optimization, power economizing in high performance designs, and reducing power in scan logic.

The session concludes with the first of two invited presentations by the Design Technology Committee, an industry EDA Users Group. The presentation is a general overview of near to mid-term requirements for physical implementation tools and flows.

7U.1 Power Gate Optimization Method for In-Rush Current and Power Up Time
Siong Kiong Teng - *Intel Corp., Bayan Lepas, Malaysia*

7U.2 CoolMe: New Techniques to Economize Power
Sumit Goswami, Vadivel Ramalingam, Milind Mahajan, Srivatsa Srinath - *Intel Corp., Bangalore, India*

7U.3 A Novel Scan Partition Technique for Controlling Power Density
Srinivas K. Vooka, **Khushboo Agarwal** - *Texas Instruments, Inc., Bangalore, India*

7U.4 INVITED: Gap Analysis of EDA Digital Implementation Tools and Flows
Martin Foltin, Hassan Naser - *Hewlett-Packard Co., Irving, TX*
David Crohn, James You - *Broadcom Corp., Irvine, CA*
Bart Martinec, Bill Read - *Freescale Semiconductor, Inc., Austin, TX*
Werner May, Werner May - *Infineon Technologies, Neubiberg, Germany*
Khankap Mounarath, Helen Xia - *Maxim Integrated Products, Inc., Dallas, TX*
Arjun Rajagopal - *Texas Instruments, Inc., Dallas, TX*
Shyam Ramji - *IBM Corp., Hopewell Junction, NY*
Ramond Rodriguez, Robert Titus - *Intel Corp., Chandler, AZ*

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Wednesday, June 8 4:00 - 6:00pm | **Verification and Test** | **Room: 30DE**

8U REAL-WORLD FUNCTIONAL VALIDATION

Chair(s):

Tor Jeremiassen - *Texas Instruments, Inc., Houston, TX*

Functional validation continues to be in the critical path for many design projects. Challenges range from capturing specifications correctly to managing huge amounts of data. This session addresses several new approaches in functional validation, including an approach for leveraging pre-silicon validation collateral in post-silicon validation, creating validation IP for PCIe using UVM, validating ECC approaches for soft errors in memories, consolidating massive amounts of coverage data, and effective deployment of SVA despite its subtle nuances.

The session concludes with the second of two invited presentations by the Design Technology Committee, an industry EDA Users Group. The presentation overviews the gaps between today's functional validation challenges and the verification tools and flows currently available.

8U.1 A Holistic Pre-To-Post Solution for Post-Si Validation of Intel SOCs

Yael Abarbanel, Eli Singerman - *Intel Corp., Haifa, Israel*
Sean Baartmans - *Intel Corp., Hillsboro, OR*

8U.2 Using the Interoperability Layer and Automation to Deliver a PCIe UVM VIP: A Successful Case Study

Anoop Kumar - *Qualcomm, Inc., Bengaluru, India*
Amit Sharma, Varun S, Abhisek Verma - *Synopsys, Inc., Bangalore, India*

8U.3 ECC Soft Errors in Memories – Effective System-Level Verification Approach

Sreenivas Machavaram, Suresh Bandaru - *LSI Corp., Bangalore, India*

8U.4 An Automated Iterative Approach to Coverage Merge

Lloyd Cha, **Christopher Hsiong** - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Vijay Akkaraju, Paul Graykowski, Padmaraj Ramachandran - *Synopsys, Inc., Mountain View, CA*

8U.5 Stumbling on SVA: Pitfalls from Real Intel Projects

Erik Seligman, Laurence Bisht, Wayne Clift - *Intel Corp., Hillsboro, OR*

8U.6 INVITED: Gap Analysis of Commercially Available Functional Verification Tools and Flows

Matthias Bauer - Infineon Technologies, Neubiberg, Germany
Thomas Dillinger - Oracle, Santa Clara, CA
Bjorn Fjellborg - Ericsson, Stockholm, Sweden
Bhadra Jay - Freescale Semiconductor, Inc., Austin, TX
Kim Joonyoung - Intel Corp., Santa Clara, CA
David Lacey - Hewlett-Packard Co., Fort Collins, CO
Jing Li - Broadcom Corp., San Jose, CA
Christopher J. Spandikow - IBM Corp., Austin, TX
Thomas Harms - Infineon Technologies, Neubiberg, Germany

Thursday, June 9 9:00 - 10:30am | **User Track** | **Room: 30DE**

9U EMBEDDED SOFTWARE IN PRACTICE

Chair(s):

Rob Aitken - *ARM, Inc., San Jose, CA*

Selecting an operating system for effective utilization in an embedded application has a wide range of commercial and open source offerings to choose from. In particular, Linux, originally designed for desktops and servers, and Android, originally designed for mobile phones, are seeing increasing adoption across a wide range of embedded applications. This session will discuss some of the key technical, system cost, development, and product life-cycle trade-offs of using RTOS technologies in embedded applications.

9U.1 INVITED: Design Considerations When Selecting an OS for ARM

Nick Lethaby - *Texas Instruments, Inc., Santa Barbara, CA*

9U.2 INVITED: Linux Graphics Meets the ARM Ecosystem

Jesse Baker - *ARM, Inc., San Francisco, CA, USA*

9U.3 INVITED: Putting Android to Work on ARC

Chris Caerts - *Synopsys, Inc., Eindhoven, The Netherlands*

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Thursday, June 9 1:00 - 2:00pm | **User Track** | **Room: OUTSIDE ROOM 33ABC**

10U POSTER SESSION

Back-End Silicon Design Topics

10U.1 Deployment of Multi-Foundry Litho Analysis and Optimization for Advanced Nodes
Kuojim Huang, Keith Thach, Joe Louis-Chandran - *Rambus, Inc., Sunnyvale, CA*
Philippe Hurat, Bala Kasthuri, Kai Lai, Sai Lee, Manoj Chacko - *Cadence Design Systems, Inc., Mountain View, CA*

10U.2 Design Analysis: The Next Leap in Convergence
Srivatsa Srinath - *Intel Corp., Bangalore, India*

10U.3 Early Layout Design Methodology and its Application to Determine Optimal Power Grid Design
Mahadevan Suryakumar, Sourav Chakravarty - *Intel Corp., Hillsboro, OR*

10U.4 EMI Reduction for LCD Panels by Using Emission Channel Model
Chiao-Chen Fang, Ying-Jiunn Lai, Yu-Wei Chen, Wang-Jin Chen, Yu-Wen Tsai - *Faraday Technology Corp., Hsin-Chu, Taiwan*

10U.5 Flexible Hierarchical Scan for Low-Power Designs
Augusli Kifli - *Faraday Technology Corp., Hsinchu, Taiwan*
Chiao-Chen Fang - *National Tsing-Hua Univ., Hsinchu, Taiwan*

10U.6 Hierarchical Timing Analysis Using Block-Level Abstraction
Kousik Debnath, Ankur Pandey, Edwin Hong Wei Yew - *Intel Corp., Folsom, CA*

10U.7 Improving Accuracy of Industry Standard Liberty Models at Non-Characterized Points Using Statistical Timing Analysis
Brian Dreibelbis, Dileep Netrabile, Hemlata Gupta, Eric Foreman, Peter Habitz, Jeffrey Hemmett - *IBM Corp., Essex Junction, VT*

10U.8 Incorporating Accurate OCV Awareness in Clock Sign-Off Flow
Drew Plant, Zakir Syed - *Infinisim, Inc., Santa Clara, CA*
Ravi Gutala, Srinivas Nori, David Larsen - *GLOBALFOUNDRIES, Dresden, Germany*

10U.9 Logic BIST Diagnosis Flow Automation Based on Combinational ATPG Tool
Andal Jayalakshmi, Tan Ewe Cheong, Amyeen Enamul - *Intel Corp., Hillsboro, OR*

10U.10 On-Chip ESD Protection Design Schematic Level Checking
Mujahid Muhammad, Nicholas Palmer, Robert Gauthier, James Montstream, Karen Henderson - *IBM Corp., Essex Junction, VT*

10U.11 OPC aware Contact/Via Position Correction
Byung-Moo Kim, Seung-Weon Paek, Hungbok Choi, Kee-Sup Kim - *Samsung, Yongin, Republic of Korea*

10U.12 Parallel Design Simulation for Neurologically Inspired Systems
Richard Schiek - *Sandia National Laboratories, Albuquerque, NM*

10U.13 Power and Area Optimized CTS for Grid Clock Distribution
Tariqul Islam, Raj Varada - *Intel Corp., Santa Clara, CA*

10U.14 Precise Substrate Noise Analysis for Power MOS Embedded LSIs
Toshiki Kanamoto, Hisato Inaba, Toshiharu Chiba, Tsukasa Matsushita, Takashi Saito - *Renesas Electronics Corp., Takasaki-shi, Japan*

10U.15 Quality Assurance Methodology of Compact MOSFET Models Including Variability Effects
Hiroo Masuda - *Renesas Electronics Corp., Tokyo, Japan*
Koutaro Hachiya - *Jedat, Inc., Tokyo, Japan*
Goichi Yokomizo - *STARC, Yokohama, Japan*

10U.16 RBO: A Tool For Timing Driven Routing and Design Closure
Li Zhuo, Nancy Y. Zhou, Chuck Alpert, Stephen Quay - *IBM Corp., Austin, TX*

10U.17 Schematic Driven Physical Verification
Ahmed Arafa, Hend Wagieh, Rami Fathy, John Ferguson, Mohamed Dessouky - *Mentor Graphics Corp., Cairo, Egypt*
Doug Morgan - *ON Semiconductor, Pocatello, ID*
Mohab H. Anis - *The American Univ. in Cairo, Cairo, Egypt*

10U.18 The High-speed Power Line Topology Check by Reducing Vias
Tomoki Kamei - *TOOL Corp., Tokyo, Japan*
Masahiro Kawakita - *Toshiba Corp., Yokohama, Japan*
Takahiro Watanabe - *Waseda Univ., Kitakyushu, Japan*

10U.19 Unified Methods for Optimizing Slow Speed Components in High Performance Designs
Andrew Spix, Raj Varada, Ragadeepika Kshatri, Sharon Martin, Archana Munshi - *Intel Corp., Santa Clara, CA*

Thursday, June 9 2:00 - 3:30pm | **Verification and Test** | **Room: 30DE**

11U CASE STUDIES IN FORMAL VERIFICATION

Chair(s):
Erik Seligman - *Intel Corp., Hillsboro, OR*

Formal verification offers the tantalizing possibility of comprehensive functional validation, but often encounters real-world limitations due to design complexity. In this session, four case studies explore industry deployment of formal verification to: check for "X"s that are observable on primary outputs, create formal specifications of micro-architectural behavior, verifying a pad ring with a specification extracted from implementation documents, and completely verify wrappers that abstract many different memory implementations.

11U.1 A Simple and Efficient X-Propagation Checking Method Based on Formal Verification
Laurent Arditi - *ARM, Ltd., Sophia Antipolis, France*
Alan Hunter - *ARM, Inc., Austin, TX*

11U.2 Applications of Formal Microarchitectural Specifications
Daryl Stewart - *ARM, Ltd., Cambridge, United Kingdom*
Alan Hunter - *ARM, Inc., Austin, TX*

11U.3 Push Button Verification of Complex Pad Ring Logic Direct from an Executable Specification
Rajkumar Ramamurti, Kritti Pathak, Olivia Wu - *Cisco Systems, Inc., San Jose, CA*

11U.4 Exhaustive Verification of Large Number of Memory Wrappers Using Formal Techniques
Normando Montecillo - *Broadcom Corp., Santa Clara, CA*
Darrow Chu - *Cadence Design Systems, Inc., San Jose, CA*

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Thursday, June 9 4:00 - 6:00pm | Analog/Mixed-Signal/RF Design | Room: 30DE

12U ADVANCED CIRCUIT DESIGN TECHNIQUES

Chair(s):

Thomas Brandtner - *Infineon Technologies, Villach, Austria*

This session discusses circuit techniques that advance design capabilities for smaller and smaller process geometries. These complex techniques extend the capabilities of existing design methods and include 3-D field simulation, low drop-out voltage regulators, correct-by-construction ESD circuit design, analog design flow, and static noise analysis.

12U.1 3-D Field Electro-Thermal Simulation of Large-Power Transistor Arrays

Dundar Dumlugöl, Wim Schoenmaker, Peter Meuris, Olivier Dupuis - *Magwel NV, Leuven, Belgium*
Edgardo Laber - *Intersil Americas, Inc., Milpitas, CA*

12U.2 Preliminary Experiments on ESD Dynamic Simulation of CDM Discharge

Remy Chevallier, Philippe Galy, Nathalie Monnet, Alexandre Dray, Ghislain Troussier, Frank Jezequel, Jean-Francois Beaumont - *STMicroelectronics, Crolles, France*

12U.3 On-Chip LDO-Aware Dynamic Voltage Drop Analysis for Large SOC Designs

Shigeru Kuriyama, Takayuki Ooshima, Genichi Tanaka - *Renesas Electronics Corp., Itami-shi, Japan*
Hiroshi Ishikawa, Kiyotaka Okuzawa, Yu Liu, Norman Chang - *Apache Design Solutions, Inc., San Jose, CA*

12U.4 A Correct-By-Construction ESD Robustness-Aware Circuit Design and Analysis Methodology Using Extended ESD Compact Models

Amol Joshi, Junjun Li, Mujahid Muhammad, John Connor, Martin Lundberg, Robert Gauthier - *IBM Corp., Essex Junction, VT*

12U.5 STARCAD-AMS: Next Generation Analog Design Flow

Kunihiko Tsuboi, Tatsuya Shirakawa, Saburo Hojo - *STARC, Yokohama-shi, Japan*

12U.6 Transistor-Level Static Noise Analysis Tool

Stephen Lim, Yoshiharu Kawamura, Mahesh Sharma - *Advanced Micro Devices, Inc., Austin, TX*

NOTES

TUTORIALS

Monday, June 6
8:30 - 10:30am, 11:30am - 1:30pm, 3:30 - 5:30pm

Additional Registration Fees apply

DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, we offer attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented multiple times to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Embedded Systems and Software **Room: 33B**

1 ANDROID APPS DEVELOPMENT BOOT CAMP

Speaker(s):

Ming Chow - *Tufts Univ., Medford, MA*

The explosive growth of the Android ecosystem has spurred great demand for developing Android applications. Not only is Android powering mobile devices, it is also powering tablets, netbooks, and appliances.

This hands-on and intensive tutorial will provide a comprehensive overview of developing Android applications using Java, Eclipse, and the Android SDK. For experienced application developers, or those who are familiar with interactive Java programming, this tutorial will provide a seamless transition to develop for the Android ecosystem. Topics that will be covered include: understanding the Android environment and the anatomy of an Android application, using the plethora of user interface elements including widgets and the map, creating views and layouts using XML, taking advantage of location-awareness and Android's rich multimedia support, using gestures and sensors including the camera, and storing data using Android data and storage APIs. Drawing, using web-based APIs, testing Android applications, and publishing to the Android Market will also be discussed.

Attendees to this tutorial should have some Java programming experience. All attendees must bring a laptop preloaded with the Eclipse IDE (current version: Helios) with the Android Eclipse Plugin, the Android SDK, and code templates which will distributed to attendees. If you have an Android-based device, it will be ideal to bring it along with the USB cable to load apps that will be developed in this tutorial.

Embedded Systems and Software **Room: 33C**

2 IPHONE APPS BEGINNER GUIDE

Speaker(s):

Patrick H. Madden - *SUNY Binghamton, Binghamton, NY*

The iPhone and iPad have revolutionized user interface design, making high resolution multi-touch displays both affordable and ubiquitous. The abundance of iOS based gadgets, coupled with a robust software development environment, has resulted in an explosion of special purpose apps.

This tutorial provides a hands-on guided tour through software development for iOS. We begin with an overview of Objective-C, the language at the core of iOS applications. We then expand to cover the key software frameworks and tools provided by the Apple XCode SDK. Small programs will be built and tested using both a software simulator and also Apple hardware. Key topics covered will include user interface construction with Interface Builder, memory management, events generated by user actions, message passing between objects, graphics frameworks, and debugging tools.

The material in the tutorial should be relevant to anyone planning to use iOS devices as displays and control interfaces to EDA tools, those developing hardware designs that might exist within an iOS powered device, and also general-purpose app developers.

Participants should have experience with software development in either C or C++ and prepare by registering with Apple (http://developer.apple.com) and installing the XCode SDK on their Mac OS laptops. Registering as a developer is free, and provides access to the SDK, extensive technical documentation, and source code to a large number of example programs.

General Interest **Room: 33A**

3 A DESIGNER'S GUIDE TO SUB-RESOLUTION LITHOGRAPHY: ENABLING THE IMPOSSIBLE TO GET TO THE 15NM NODE

Speaker(s):

Lars Liebmann - *IBM Corp., Fishkill, NY*
Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*

Optical lithography, for three decades, the workhorse of semiconductor scaling, has run out of steam. While previous technology nodes where enabled primarily by exposure wavelength reduction, this source of resolution scaling hit a wall in the 90nm technology node. All subsequent density improvements, baring a brief reprieve with the introduction of immersion lithography, are being enabled by computational scaling techniques. The ability of these computational solutions to scale past one fundamental resolution limit after another has been instrumental in maintaining the industry roadmap for six technology generations. However, these computational scaling techniques come at the price of increasingly complex physical design, more severe design restrictions, and a need for deeper design and process co-optimization.

This short course will introduce the attendee to the principles of lithography scaling, explain the fundamental resolution limits and computational techniques implemented to overcome them, and help develop a thorough understanding of the increasingly severe design implications of sub-resolution patterning as we push towards the 15nm technology node. For every major resolution domain, the course will focus on both the manufacturing process characteristics as well as the physical verification characteristics of the applicable technology nodes, helping the attendee appreciate the technical basis for the increasingly complex EDA solutions that continue to be implemented. Wherever applicable, examples of existing computational scaling tools will be shown and a CD will be provided to participants containing example layouts and basic physical verification rules for each technology node in discussion.

TUTORIALS

Monday, June 6
8:30 - 10:30am, 11:30am - 1:30pm, 3:30 - 5:30pm

Additional Registration Fees apply

DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, we offer attendees a set of two-hour intense introductions to specific topics. Each tutorial will be presented multiple times to allow attendees to cover multiple topics. If you register for tutorials, you have the option to select three out of the six topics.

Emerging Technologies **Room: 29CD**

4 DEMYSTIFYING TSV-BASED 3-D STACKED ICS - A DESIGN AND TEST PERSPECTIVE

Speaker(s):

Paul Franzon - *North Carolina State Univ., Raleigh, NC*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

After years of research and development, Through-silicon vias (TSVs) are becoming a manufacturing reality. Soon, a wave of new TSV-based 3-D stacked ICs (and 22½ stacked ICs) will hit the market, including CMOS image sensors, memory cubes, stacked FPGAs, memory-on-logic, and logic-on-logic. This tutorial starts off with an introduction of TSV-based 3-D technologies and overview of its motivation, benefits, and application drivers. Subsequently, it discusses the opportunities as well as challenges related to this new technology in architecture, design, design-for-test, and test. Numerous practical examples are used to illustrate how engineers get by today to create their 3-D products and what tools they ideally would work with in the near and mid-term future. Standardization efforts will also be discussed. After this tutorial, you will have sufficient knowledge to assess what 3-D technology means for you!

Intended Audience:

Architects, front-end and back-end designers, design-for-test, and test engineers of integrated circuits and systems and their managers; also researchers, design methodology developers, EDA engineers, test methodology developers, and test tool developers.

Low-Power Design **Room: 30C**

5 SYSTEM-LEVEL DESIGN AND SOFTWARE DEVELOPMENT FOR ENERGY EFFICIENT PLATFORMS: CHALLENGES FROM MODELS TO METHODS

Speaker(s):

Alan Gibbons - *Synopsys, Inc., Reading, United Kingdom*
David Flynn - *ARM, Ltd., Cambridge, United Kingdom*
Achim NOhl - *Synopsys, Inc., Aachen, Germany*

"I upgraded my phone's software and battery life dropped by 50%." Internet flame, or real possibility?

This tutorial is a quick start for everyone interested in the current state of energy efficient system level design, from IP power characterization and modeling up to, and including, the development of application software. Particular attention is given to virtual prototyping for use in software centric power analysis and optimization.

Attendees will gain an understanding of the behavior of virtual prototype models, how this behavior can be tuned to provide insight into real device performance and how software analysis and debug tools allow for a top down system level root cause analysis of power inefficiencies and power defects. Attendees will have an opportunity to examine a complete virtual prototype model and observe the power impact of changes in hardware and software.

Specific attention given to:

Power-aware software design and optimization: providing the software development team the ability to make intelligent power-aware decisions and optimization during development while emulating real hardware.

Design and optimization of complex power control schemes including the integration of distributed and centralized power control, interactions between hardware power control and the OS Power Management (OSPM), as well as the software bring-up of power management units enabling the co-design of both the hardware and software aspects of power management within the full system context.

Target audience includes engineers who develop energy efficient platforms for mobile applications, as well as hardware and software developers for today's mobile internet devices.

Interconnect and Reliability **Room: 32AB**

6 STARTER KIT FOR CHIP-TO-SYSTEM RELIABILITY

Speaker(s):

Nematollah Bidokhti - *Cisco Systems, Inc., San Jose, CA*
Mohammad Tehranipoor - *Univ. of Connecticut, Storrs, CT*
Bill Eklow - *Cisco Systems, Inc., San Jose, CA*

For a long time, reliability has been an after thought, but with technology scaling, power, thermal speed, complexity, time-to-market, and cost there will be a significant impact on device and product reliability going forward. Given this "perfect technology storm," it is imperative today that engineers understand the impact of these influences on product reliability and become more proactive in identifying and addressing reliability risks in the design. The engineers/companies that are reactive will pay significantly; not only in terms of dollars, but also in terms of customers.

This tutorial will cover the "fundamental" concepts around component and system reliability, including: definition of key terms, current and future challenges in reliability, tools, methodologies and processes for identifying reliability risks, and case studies demonstrating problems and solutions.

This tutorial is meant for participants who are either beginners, or have limited reliability engineering background, and require an additional refresher with the latest development in this area. It provides an up-to-date understanding of future reliability and verification challenges and offers a set of best practices to address them. We will present: (1) novel methodologies to analyze reliabilities at different level of OS abstraction, (2) case studies to help understanding the impact of technology scaling and system complexity on reliability, (3) pre-tapeout methodologies to perform better margining for reliability, and (4) post-silicon, self-healing, and calibration methodologies.

In addition, the tutorial will include the current and future potential areas for reliability automation and robustness. The attendee will come out of the tutorial with a better understanding and a set of tools to proactively mitigate any reliability risks.

WORKSHOPS

Additional Registration Fees apply

Sunday, June 5 8:30am - 5:30pm | **Interconnect and Reliability** | **Room: 33C**

DAC WORKSHOP ON DIAGNOSTIC SERVICES IN NETWORK-ON-CHIPS: TEST, DEBUG, AND ON-LINE MONITORING

Moderator(s):
Qiang Xu - *The Chinese Univ. of Hong Kong, Hong Kong, China*

Organizer(s):
Thilo Pionteck - *Univ. zu Lübeck, Lübeck, Germany*
Li Li - *Nanjing Univ., Nanjing, China*
Partha Pratim Pande - *Washington State Univ., Pullman, WA*

Speaker(s):
Bill Penner - *Intel Corp., DuPont, WA*
Christof Teuscher - *Portland State Univ., Portland, OR*
Han Yinhe - *Chinese Academy of Sciences, Beijing, China*
Amlan Ganguly - *Rochester Institute of Technology, Rochester, NY*
Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

This Workshop will include a Panel, featuring:
Qiang Xu - *The Chinese Univ. of Hong Kong, Hong Kong, China*
Fabien Clermidy - *CEA-Leti, Grenoble, France*
Saeed Shamshiri - *Univ. of California, Santa Barbara, CA*
W. Rhett Davis - *North Carolina State Univ., Raleigh, NC*

Network-on-Chips (NOCs) are settling as a new on-chip communication paradigm. Diagnostic services, such as test, debug, and on-line monitoring, are becoming an important factor in designing next-generation NOC-based systems, especially when going to 3D NOC designs. The NOC infrastructure itself requires diagnostic services, and can also be used to support those for the entire system. Although significant research has been done in NOC design, there are many open and pressing issues regarding diagnostic services. The focus of this workshop is to explore them and their implications on system design.

The workshop program will contain keynote and invited talks from industry and research, paper and poster sessions as well as a panel discussion. This year's focus will be set on test, debug and on-line monitoring of 3-D Network-on-Chips. DSNOC'11 is the fifth edition a sequence of successful events hosted by DATE in 2007 and 2009, and DAC in 2008 and 2010.

Sunday, June 5 9:00am - 5:00pm | **Embedded Systems and Software** | **Room: 30C**

DAC WORKSHOP ON DESIGN, ANALYSIS, AND IMPLEMENTATION OF REAL-TIME SYSTEMS WITH TIME-TRIGGERED AND EVENT-TRIGGERED APPLICATIONS

Chair(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Organizer(s):
Arkadeb Ghosal - *National Instruments Corp., Berkeley, CA*
Kaushik Ravindran - *National Instruments Corp., Berkeley, CA*

Speaker(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Hermann Kopetz - *Technische Univ. Wien, Vienna, Austria*
Raj Rajkumar - *Carnegie Mellon Univ., Pittsburgh, PA*
Wolfgang Pree - *Univ. Salzburg, Salzburg, Austria*
Claudio Pinello - *United Technologies, Berkeley, CA*
Hugo Andrade - *National Instruments Corp., Berkeley, CA*
Stavros Tripakis - *Univ. of California, Berkeley, CA*
Stephen Neuendorffer - *Xilinx, Inc., Berkeley, CA*
José Luis Pino - *Agilent, Westlake Village, CA*

In recent years, interest in determinacy, portability, and composability of real-time systems have led to a significant research effort in time-triggered models. Although the time-triggered model of computation can capture the above properties, the model may be too constrained to reflect real-world requirements. This often leads to conservative implementation, over utilization of resources, and high cost of development. A more flexible model is time-triggered tasks overlaid with event-triggered tasks. One example of such a model is the FlexRay communication protocol for automotive embedded systems that allows time-triggered and event-triggered message communication. This workshop will focus on industrial case studies, models of computation, analysis methodologies, and integrated development platforms for mixed-triggered systems.

Sunday, June 5 9:00am - 6:00pm | **Emerging Technologies** | **Room: 29AB**

DAC WORKSHOP ON PARALLEL ALGORITHMS, PROGRAMMING, AND ARCHITECTURES (PAPA)

Organizer(s):
Rasit Onur Topaloglu - *GLOBALFOUNDRIES, Milpitas, CA*

Speaker(s):
Jason Cong - *Univ. of California, Los Angeles, CA*
Peng Li - *Texas A&M Univ., College Station, TX*
Hai Zhou - *Northwestern Univ., Evanston, IL*
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*
Bevan Baas - *Univ. of California, Davis, CA*
Lei He - *Univ. of California, Los Angeles, CA*
Sunita Chandrasekaran - *Univ. of Houston, Houston, TX*
Richard Vuduc - *Georgia Institute of Technology, Atlanta, GA*
Paulius Micikevicius - *NVIDIA Corp., Santa Clara, CA*

This Workshop will include a Panel, featuring:
Tom Spyrou - *Cadence Design Systems, Inc., San Jose, CA*
Duaine Pryor - *Mentor Graphics Corp., Fremont, CA*
Benedict R. Gaster - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Paulius Micikevicius - *NVIDIA Corp., Santa Clara, CA*
Ramki Balasubramanian - *Synopsys, Inc., Mountain View, CA*
One additional panelist will include a member from Intel Corp.

We have an exciting new workshop at the Design Automation Conference in San Diego on June 5, 2011. Our workshop contains invited talks from prominent names in the field.

The primary goal of the workshop is to bring together three main categories of parallelism researchers to improve the understanding of progress and open problems in the cross-coupled fields of programming, algorithms, and architectures. The conference also serves the electronic design automation community to facilitate discussions towards better understanding the most recent algorithms, languages, and architectures. For a summary of sample topics and most up to date schedule of talks and program, please visit our website: www.papaworkshop.com

We hope to see you at our workshop in "America's Finest City," San Diego.

WORKSHOPS

Additional Registration Fees apply

Sunday, June 5 8:00am - 5:00pm | **Embedded Systems and Software** | **Room: 29CD**

DAC WORKSHOP ON INTRA AND INTER-VEHICLE NETWORKING: PAST, PRESENT, AND FUTURE

Chair(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Organizer(s):
Paolo Giusto - *General Motors Company, Palo Alto, CA*
Haibo Zeng - *General Motors Company, Palo Alto, CA*
Arkadeb Ghosal - *National Instruments Corp., Berkeley, CA*

Speaker(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Raj Rajkumar - *Carnegie Mellon Univ., Pittsburgh, PA*
Flavio Bonomi - *Cisco Systems, Inc., San Jose, CA*
Wilfried Steiner - *TTTech, Vienna, Austria*
Markus Kuehl - *aquintos GmbH, Karlsruhe, Germany*
Harald Gall - *austriamicrosystems AG, Unterpremstaetten, Austria*
Frank Schirrmeister - *Synopsys, Inc., Mountain View, CA*
Rodney Cummings - *National Instruments Corp., Austin, TX*
Markus Jochim - *General Motors Company, Warren, MI*
Bill Chown - *Mentor Graphics Corp., Wilsonville, OR*
Arthur Marris - *Cadence Design Systems, Inc., Livingston, United Kingdom*
Robert Juliano - *Mirabilis Design Inc., Sunnyvale, CA*
Marek Jersak - *Symtavision GmbH, Braunschweig, Germany*

Market demands and regulations are leading the automotive industry to face increasing design and business challenges due to the fast adoption rates of sophisticated infotainment, advanced safety features, semi-autonomous driving/control, and remote diagnostics. Specifically, requirements for efficient, fast, and reliable communications among modules within a vehicle and between vehicles in a fleet are testing the limits of current network protocols. Existing networking technologies (e.g., CAN, FlexRay) for intra-vehicle communication, and RADAR/LIDAR, camera-based, inter-vehicle sensing may not be able to tackle all the challenges on bandwidth, cost, and reliability. Hence, new protocols for intra-vehicle, vehicle-to-vehicle, and vehicle-to-infrastructure communications must be defined and developed to facilitate the adoption of new features for enhanced safety, driver comfort, and commercial use cases. This workshop focuses on the past, present, and potential future landscape of intra and inter-vehicle communication technologies, including CAN, FlexRay, Ethernet, and DSRC, with emphasis on the potential opportunities for the EDA industry in providing tool support for the analysis and design of Ethernet and DSRC based automotive architectures. Starting from the automotive OEM's requirements for the new technologies and the related tools to facilitate the adoption of new features, the workshop will also focus on the academic research efforts in this area as well as on the technologies and tool providers therein.

Sunday, June 5 10:00am - 6:00pm | **System-Level Design** | **Room: 33B**

DAC WORKSHOP ON USING THE POWER OF THE SYSTEMC AMS EXTENSIONS

Organizer(s):
Martin Barnasconi - *NXP Semiconductors, Eindhoven, The Netherlands*

Speaker(s):
Karsten Einwich - *Fraunhofer IIS, Dresden, Germany*
François Pêcheux - *Univ. Pierre et Marie Curie, Paris, France*
Christoph Grimm - *Technische Univ. Wien, Vienna, Austria*
Martin Barnasconi - *NXP Semiconductors, Eindhoven, The Netherlands*

Today's embedded systems interact more and more tightly with the analog physical environment; where digital HW/SW subsystems become functionally interwoven with analog/mixed-signal (AMS) blocks such as RF interfaces, power electronics, or sensors and actuators. Examples are software defined radios, sensor networks, automotive applications, or systems for image sensing. This requires new means to model and simulate the interaction between AMS subsystems and HW/SW subsystems at functional and architecture levels. Especially for this purpose, the SystemC language standard has been extended with powerful AMS capabilities to tackle the challenges in heterogeneous electronic system-level (ESL) design.

This workshop targets hardware and system engineers, integrators, architects, and verification engineers active in industrial projects where analog and digital functionality comes together and where interoperability between AMS and HW/SW subsystems becomes apparent. The workshop will explain the power of the SystemC AMS extensions and will bring hands-on experience to show how to efficiently use SystemC AMS for mixed-signal, system-level design, and verification tasks.

This event will be conducted as a true *work*shop: after a basic introduction on the new SystemC AMS modeling concepts and methodology, everyone is encouraged to actually create some basic examples by using the SystemC AMS proof-of-concept implementation. To facilitate this, a CD distribution will be made available for the attendees, including a fully prepared mixed-signal ESL design environment, which they can run immediately on their own laptop. In an interactive way, presentations and "labs" will be alternated, giving attendees a good understanding of the power of using the SystemC AMS extensions, which they can apply in their daily work.

Sunday, June 5 10:00am - 1:00pm | **General Interest** | **Room: 33A**

DAC WORKSHOP ON UNIVERSAL VERIFICATION METHODOLOGY (UVM) - VERIFYING BLOCKS TO IP TO SOCS AND SYSTEMS

Organizer(s):
Yatin Trivedi - *Synopsys, Inc., Mountain View, CA*
Dennis Brophy - *Mentor Graphics Corp., Wilsonville, OR*
Stanley Krolikoski - *Cadence Design Systems, Inc., San Jose, CA*

Speaker(s):
Janick Bergeron - *Synopsys, Inc., Mountain View, CA*
Tom Fitzpatrick - *Mentor Graphics Corp., Groton, MA*
John Fowler - *Advanced Micro Devices, Inc., Austin, TX*
Hillel Miller - *Freescale Semiconductor, Inc., Austin, TX*
Sharon Rosenberg - *Cadence Design Systems, Inc., San Jose, CA*
Ambar Sarkar - *Paradigm Works, Inc., Andover, MA*

The Accellera Verification IP Technical Subcommittee (VIP-TSC), building on over two years of work by verification experts from around the world, released Universal Verification Methodology (UVM) in February 2011. This workshop, presented by expert verification methodology architects and engineers, will provide an example-based overview of UVM to chip and SOC design and verification engineers of all skill levels on the first open-source verification methodology to be fully supported and endorsed by all major EDA vendors, and many end-user and consulting companies.

We will begin with motivation for UVM and provide an introduction to many of the fundamental concepts in UVM. This will be followed by a walk-through of the key features to build a verification environment including stimulus generation and test shutdown. We will then present the TLM communication mechanisms, including TLM2 in UVM.

Next, we will focus on UVM component and environment control, including run-time phase management. We will continue with a discussion of the UVM register package, including how to create and manage stimulus and checking at the register level. The workshop will conclude with a review of all of the topics, showing how they fit together in a complex SOC verification environment.

WORKSHOPS

Additional Registration Fees apply

Monday, June 6 - Tuesday, June 7 9:00am - 6:00pm | **Bio Design Automation** | **Room: 28AB**

DAC WORKSHOP ON INTERNATIONAL WORKSHOP ON BIO-DESIGN AUTOMATION (IWBDA)

Organizer(s):

Douglas Densmore - *Boston Univ., Boston, MA*
Leonidas Bleris - *Univ. of Texas at Dallas, Richardson, TX*
Xiling Shen - *Cornell Univ., Ithaca, NY*
Smita Krishnaswamy - *Columbia Univ., New York, NY*
Jacob Beal - *BBN Technologies, Cambridge, MA*
Jonathan Babb - *Massachusetts Institute of Technology, Cambridge, MA*
Natasa Miskov-Zivanov - *Univ. of Pittsburgh, Pittsburgh, PA*

Speaker(s):

Adam Arkin - *Univ. of California, Berkeley, CA*
Erik Winfree - *California Institute of Technology, Pasadena, CA*
Christopher Voigt - *Univ. of California, San Francisco, CA*

The International Workshop on Bio-Design Automation (IWBDA) brings together researchers from the synthetic biology, systems biology, and design automation communities. The focus is on concepts, methodologies, and software tools to enable the computational analysis of biological systems and the synthesis of biological functions. Still in its early stages, the field of synthetic biology has been driven by experimental expertise; much of its success can be attributed to the skill of the researchers in specific domains of biology. There has been a concerted effort to assemble repositories of standardized components. However, creating and integrating synthetic components remains an ad-hoc process. The field has now reached a stage where it calls for computetr-aided design tools.

The electronic design automation (EDA) community has unique expertise to contribute to this endeavor. This workshop offers a forum for cross-disciplinary discussion, with the aim of seeding collaboration between the research communities.

Wednesday, June 8 1:00 - 4:00pm | **Emerging Technologies** | **Room: 25ABC**

DAC WORKSHOP ON BUILDING BLOCKS FOR SCALABLE CLOUD SYSTEMS

Organizer(s):

Manish Pandey - *Synopsys, Inc., Mountain View, CA*
Andreas Kuehlmann - *Coverity, Inc., San Francisco, CA*

Speaker(s):

Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*
Kazi A. Zaman - *Yahoo!, Inc., Sunnyvale, CA*
Frank Weigel - *Couchbase, Mountain View, CA*

This workshop will introduce the building blocks of large-scale cloud computing to the design automation community. Tremendous advances have been made in the creation of new EDA technologies to design complex multi-billion transistor chips. However, EDA software tools are still built as monolithic software components that only recently have started building parallelism into the software, with multi-threaded implementations on multi-core processor systems. In contrast, the software systems run by companies such as Yahoo, Google, and Facebook employ building blocks that are designed from the ground-up to be highly distributed and scalable. These building blocks perform distributed computation (Map-Reduce, Hadoop), distributed key-value databases (Membase, NoSQL), distributed storage (Hadoop Distributed File System, Google File System), and run on hundreds to thousands of machines.

The workshop will start with an overview on the evolution of scalable systems which have evolved into massive clusters with commodity components and the new paradigm of Data-Intensive Scalable Computing. It will be followed by presentations on Hadoop, an open source implementation of Map-Reduce, Membase, an open source distributed, key-value database management system, and distributed file systems that provide a storage framework for these large distributed data-intensive applications. The presentations will cover these technologies and their applications to inspire innovative ways of building new design automation solutions.

Thursday, June 9 8:30am - 5:30pm | **General Interest** | **Room: 25ABC**

DAC WORKSHOP ON SMART GRID AND DESIGN AUTOMATION II

Organizer(s):

David Kung - *IBM Corp., Yorktown Hts, NY*
Doug Houseman - *EnerNex Corp., Knoxville, TN*
Jinjun Xiong - *IBM Corp., Yorktown Hts, NY*

Speaker(s):

Maria Ilic - *Carnegie Mellon Univ., Pittsburgh, PA*
Doug Houseman - *EnerNex Corp., Knoxville, TN*
Ian Hiskens - *Univ. of Michigan, Ann Arbor, MI*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Yiyu Shi - *Missouri Univ. of Science and Technology, Rolla, MO*
Dennis Eccleston - *New York Power Authority, White Plains, NY*

The Smart Grid and Design Automation II workshop is a follow up to the "Workshop on the Synergies Between DA and Smart Grid" in DAC 2010.

The workshop in 2010 served the purpose of introducing the DA and Power Energy communities to each other and providing a forum for exchange of domain knowledge between the two respective disciplines. This follow-up workshop will further strengthen the ties between the two communities and provide in-depth insights on potential Smart Grid research areas, with specific emphasis on computational challenges.

The workshop will be featuring leaders from the Power Energy industry and academia, who will present the challenges they are facing and the current activities in their organizations. Domain experts will lecture on topics that are of interest to the DA community, such as the challenges of a 2-way grid and distributed generation, the limits of the current infrastructure and what it should evolve into, the change in consumer habits and demand response, and the simulation and analysis tools used by the industry.

We will also sample selective research topics on the Smart Grid from Design Automation researchers who have ventured into the Power Energy domain.

Additional Registration Fees apply

Thursday, June 9 8:30am - 5:00pm | Embedded Systems and Software | Room: 24AB

DAC WORKSHOP ON MULTIPROCESSOR SYSTEM-ON-CHIP FOR CYBER PHYSICAL SYSTEMS: PROGRAMMABILITY, RUN-TIME SUPPORT, AND HARDWARE PLATFORMS FOR HIGH PERFORMANCE EMBEDDED APPLICATIONS

Organizer(s):

Michael Hübner - *Karlsruher Institut für Technologie, Karlsruhe, Germany*
Jörg Henkel - *Karlsruher Institut für Technologie, Karlsruhe, Germany*
Diana Göhringer - *Fraunhofer IOSB, Ettlingen, Germany*

Speaker(s):

Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Jürgen Becker - *Karlsruher Institut für Technologie, Karlsruhe, Germany*
Dac Pham - *Freescale Semiconductor, Inc., Austin, TX*
Hiren D. Patel - *Univ. of Waterloo, Waterloo, ON, Canada*
Rajesh K. Gupta - *Univ. of California at San Diego, La Jolla, CA*
Lothar Thiele - *ETH Zürich, Zuerich, Switzerland*
Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Robert Dick - *Univ. of Michigan, Ann Arbor, MI*

Cyber physical systems combine the system's computational with the physical elements. This type of systems can often be found in embedded systems of various domains like aerospace, automotive, chemical processes, civil infrastructure, energy, healthcare, manufacturing, transportation, entertainment, and consumer appliances. Since applications in this domains require a high computational performance, novel approaches for the computing elements have to be provided. Multicore hardware is a promising solution to provide the sufficient performance/power consumption ratio. Multicore architectures offer a better performance/Watt ratio than single core architectures with similar performance. Combining multicore and coprocessor technology promise extreme computing power for highly CPU-time-consuming applications. Especially, FPGA-based accelerators not only offer the opportunity to speedup an application by implementing their compute-intensive kernels into hardware but also to adapt to the dynamical behavior of an application.

The purpose of the third edition of this very successful workshop is to evaluate strategies for future system design in MPSoC architectures, especially for cyber physical systems. Both aspects, hardware design and tool-integration into existing development tools will be discussed. Especially, the novel trends in MPSoC combined with reconfigurable architectures are a topic in this workshop. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

The workshop speakers are invited to submit a paper to the Special Issue of the ACM Transactions on Embedded Computing Systems (TECS) which is organized in conjunction to this workshop.

WORK-IN-PROGRESS (WIP)

Wednesday, June 8 6:00 - 7:00pm | **General Interest** | **Sails Pavilion**

POSTER SESSION

Organizer(s):
Nikil Dutt - *Univ. of California, Irvine, CA*
Soha Hassoun - *Tufts Univ., Medford, MA*

New this year to the DAC program is the Work in Progress (WIP) poster session. This session is designed to provide authors an opportunity to present their ideas to industry peers in an effort to initiate discussion and gain feedback in the early stages of the project.

56.1 Hybrid CMOS-MQCA Logic Architecture Using Multi-Layer Spintronic Devices

Jayita Das, Sanjukta Bhanja, Srinath Rajaram - *Univ. of South Florida, Tampa, FL*
Syed M. Alam - *Everspin Tech., Inc., Austin, TX*

56.2 A Parametric Model Order Reduction Approach for Weakly Nonlinear Systems

Ehsan Rasekh, Anestis Dounavis - *The Univ. of Western Ontario, London, ON, Canada*

56.3 Statistical Model of TiO2 Memristor

Hai Li, Miao Hu - *Polytechnic Institute of New York Univ., Brooklyn, NY*
Yiran Chen - *Univ. of Pittsburgh, Pittsburgh, PA*
Robinson E. Pino - *Air Force Research Laboratory/RITC, Rome, NY*

56.4 Unequal RF Interconnected Wireless Network-On-Chip to Improving On-Chip Communication Performance

Danella Zhao, **Ruizhe Wu** - *Univ. of Louisiana at Lafayette, LA*

56.5 An Efficient Methodology of Topology Selection and Sizing in Geometric Programming-Based Design Environment

Supriyo Maji, Pradip Mandal - *Indian Institute of Technology, Kharagpur, India*

56.6 A Heterogeneous On-Demand Load-Balanced Cloud-Ground System with Special Emphasis on Functional Verification Applications

Swapnajit Mitra - *PLX Technology Inc., Sunnyvale, CA*
Kiran Maiya - *Synopsys, Inc., Mountain View, CA*

56.7 Post-Manufacturing Instruction Synthesis for Adaptive Embedded Processor System

Yong Kyu Jung - *Adaptmicrosys, LLC and Gannon Univ., Erie, PA*

56.8 Learning Digital Circuits: Initial Results

Bo Marr - *Raytheon Company, Manhattan Beach, CA*

56.9 A Highly Energy-Efficient Accelerator Enabling Post-Silicon Engineering Changes and Its Patch Compilation Method

Hiroaki Yoshida, Masahiro Fujita - *The Univ. of Tokyo, Tokyo, Japan*

56.10 Single-Copy L1-NUCA for Cache Capacity Maximization in Multicore SOC

Chien-Chih Chen, Tien-Fu Chen - *National Chiao Tung Univ., HsinChu, Taiwan*
Yin-Chi Peng, Chi-Neng Wen, Shu-Husan Chou - *National Chung Cheng Univ., Chia-Yi, Taiwan*

56.11 VBON: Towards Efficient On-Chip Networks Via Hierarchical Virtual Bus

Libo Huang, Zhiying Wang, Nong Xiao - *National Univ. of Defense Technology, Changsha, China*

56.12 A Cycle-Level SIMT-GPU Simulator Framework

Chia-Lin Yang, Yu-Jung Cheng, Chien-Wei Lo, Po-Han Wang - *National Taiwan Univ., Taipei, Taiwan*

56.13 Model-Based Concolic Testing for Embedded Software

Giuseppe Di Guglielmo, Franco Fummi, Graziano Pravadelli, Stefano Soffia - *Univ. di Verona, Verona, Italy*
Masahiro Fujita - *The Univ. of Tokyo, Tokyo, Japan*

56.14 Block-Level 3-D IC Design with Through-Silicon-Via Planning

Dae Hyun Kim, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*
Rasit O. Topaloglu - *GLOBALFOUNDRIES, Santa Clara, CA*

56.15 Controllability Improved Hierarchical Trajectory Piecewise-Linear Macromodeling Approach

Xiaoda Pan, **Xuan Zeng**, Fan Yang - *Fudan Univ., Shanghai, China*

56.16 System-Level Contracts for Composition in Analog Platform-Based Design

Alberto Puggelli, Xuening Sun, Pierluigi Nuzzo, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

56.17 Optimal Layout Decomposition for Double Patterning Technology

Xiaoping Tang - *IBM Corp., Yorktown Heights, NY*
Minsik Cho - *IBM T.J. Watson Research Ctr., Yorktown Heights, NY*

56.18 Design and Optimization of Magnetic-Electrical Interfaces for NML Circuit Output

Shiliang Liu, Xiaobo Sharon Hu, Michael T. Niemier, Joseph J. Nahas, Gary H. Bernstein, Wolfgang Porod - *Univ. of Notre Dame, South Bend, IN*

56.19 The Power Cost of Over-Designing Codes

Karthik Ganesan, Pulkit Grover - *Univ. of California, Berkeley, CA*

56.20 Workload-Aware Throughput Optimization of Power-Constrained GPGPUs

Vijay Sathish, Jungseob Lee, Nam Sung Kim, Katherine Compton - *Univ. of Wisconsin, Madison, WI*
Mike Schulte - *Advanced Micro Devices, Inc., Texas, WI*

56.21 Analyzing High Dimensional Robust Stability Distribution of Linear Analog Circuits Via Routh Criterion and Interval Arithmetic

Xuan Zeng, **Changhao Yan** - *Fudan Univ., Shanghai, China*
Shengguo Wang - *Univ. of North Carolina, Charlotte, NC*

56.22 MCSL: A Realistic Traffic Benchmark Suite for Network-On-Chip Studies

Weichen Liu, **Jiang Xu**, Xuan Wang, Xiaowen Wu, Yaoyao Ye, Mahdi Nikdast, Zhehui Wang - *Hong Kong Univ. of Science and Technology, Kowloon, Hong Kong*
Wei Zhang - *Nanyang Technological Univ., Singapore, Singapore*

56.23 Electromigration Modeling and Full-Chip Reliability Analysis for TSV-Based 3-D ICs

Mohit Pathak, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*
Jiwoo Pak, David Z. Pan - *Univ. of Texas, Austin, TX*

56.24 Logic Bist Post-Silicon Diagnosis Solution for Unit-Level Logid Diagnosis

Andal Jayalakshmi, Tan Ewe Cheong, Amyeen Enamul - *Intel Corp., Hillsboro, OR*

WORK-IN-PROGRESS (WIP)

Wednesday, June 8 6:00 - 7:00pm | **General Interest** | **Sails Pavilion**

56.25 An Architectural Countermeasure Against Power Analysis Attacks for FSR-Based Stream Ciphers

Shohreh Sharif Mansouri - *Kungliga Tekniska Högskolan, Stockholm, Sweden*
Elena Dubrova - *Royal Institute of Technology, Kista, Sweden*

56.26 Online Skew Tuning for Timing Speculation

Rong Ye, Qiang Xu, Feng Yuan - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

56.27 Backside GND Plug: A Superior Technology to Mitigate TSV-Induced Substrate Noise in 3-D ICs

Nauman Khan - *Tufts Univ., Medford, MA*

56.28 How Sensitive is Processor Customization to the Workload's Input Datasets?

Maximilien Breughe, Lieven Eeckhout, Stijn Eyerman - *Ghent Univ., Gent, Belgium*
Zheng Li, Olivier Temam - *INRIA, Orsay, France*
Yang Chen - *Tsinghua Univ., Beijing, China*
Chengyong Wu - *Institute of Computing Tech., Beijing, China*

56.29 Autonomous Power Management Technique for Communication Systems

Muhammad S. Khairy, Ahmed Eltawil, Fadi Kurdahi - *Univ. of California, Irvine, CA*
Amin Khajeh - *Univ. of California Irvine and Qualcomm, Inc., Austin, TX*

56.30 VLSI Characterization of NIST SHA-3 Finalists

Xu Guo, Meeta Srivastav, Sinan Huang, Leyla Nazhandali, Patrick R. Schaumont - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

56.31 Energy-Optimized Mapping of Application to Smartphone Platform – A Case Study of Mobile Face Recognition

Yi-Chu Wang, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*

56.32 Automatic SET propagation Tool Based on Analytical Model

Salvador Barcelo, Xavier Gili, Sebastià Bota, Jaume Segura - *Univ. de les Illes Balears, Palma de Mallorca, Spain*

56.33 Hybrid Dynamic Thermal Management for Embedded Heterogeneous MPSOCs with Special Purpose IP Cores

Yen-Kuan Wu, Shervin Sharifi, Tajana Simunic Rosing - *Univ. of California at San Diego, La Jolla, CA*

56.34 A High-Level Benchmarks Generator for Multicore Platforms Running Real-Time Applications

Joffrey Kriegel, Florian Broekaert - *Thales Communications, Inc., Colombes, France*
Alain Pegatoquet, Michel Auguin - *Université de Nice Sophia Antipolis, Valbonne, France*

56.35 Modeling and Analysis of Circuits for Approximate Computing

Rangharajan Venkatesan, Amit Agarwal, Anand Raghunathan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

56.36 Statistical Characterization of Chip Power Behavior at Post-Fabrication Stage

Ankur Srivastava, Yufu Zhang, Bing Shi - *Univ. of Maryland, College Park, MD*

56.37 A New Voltage Binning Technique for Yield Improvement Based on Graph Theory

Ruijing Shen, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*
Zhigang Hao - *Shanghai Jiao Tong Univ., Shanghai, China*

56.38 Viability Analysis Under Delay Variation

Taewhan Kim, Jongyoon Jung - *Seoul National Univ., Seoul, Republic of Korea*

56.39 Implementing the Practical Chip-Package-Board Codesign Considering Package Design and Board-Escape Routing

Ren-Jie Lee - *National Chiao Tung Univ. and Novatek Microelectronics Corp., Hsinchu, Taiwan*
Hsin-Wu Hsu - *National Chiao Tung Univ. and Global Unichip Corp., Hsinchu, Taiwan*
Hung-Ming Chen - *National Chiao Tung Univ., Hsinchu, Taiwan*

56.40 A Low-Overhead Hardware-Software Collaborated Approach for Soft-Error Tolerance

Jiang Xu, Weichen Liu, Xuan Wang, Xiaowen Wu, Yaoyao Ye, Mahdi Nikdast - *Hong Kong Univ. of Science and Technology, Kowloon, Hong Kong*
Yu Wang - *Tsinghua Univ., Beijing, China*
Wei Zhang - *Nanyang Technological Univ., Singapore, Singapore*

56.41 A Data-Driven Modeling Approach to Stochastic Computation for Low-Energy Biomedical Devices

Shoaib Mohammed, Kyong Ho Lee, Kuk J. Jang, Naveen Verma - *Princeton Univ., Princeton, NJ*
Ali H. Shoeb - *Massachusetts General Hospital, Boston, MA*

56.42 Scalable Floorplanning

Nimish Shah, Renshen Wang - *Mentor Graphics Corp., Fremont, CA*

56.43 DWARV: A HDL Compiler with Support for Scheduling Custom IP Blocks

Razvan Nane, Vlad Mihai Sima, Koen Bertels - *Delft Univ. of Technology, Delft, The Netherlands*
Hans Van Someren - *ACE Associated Computer Experts bv, Amsterdam, The Netherlands*

56.44 uIFTL: A Novel FTL with Fully-Utilized Log Blocks for MLC NAND Flash Memory Storage Systems

Zili Shao, Zhiwei Qin, Yi Wang - *The Hong Kong Polytechnic Univ., Kowloon, Hong Kong*
Guohui Wang, Yong Guan - *Capital Normal Univ., Beijing, China*

56.45 Routing Wire Optimization Through Generic Synthesis on FPGA Carry Chains

Hadi Afshar - *Ecole Polytechnique Fédérale de Lausanne, Switzerland*

56.46 A Multi-Threaded, Coarse-Grained Array Processor for Wireless Baseband

Tom Vander Aa, Martin Palkovic, Matthias Hartmann, Praveen Raghavan, Antoine Dejonghe, Liesbet Van der Perre - *IMEC, Leuven, Belgium*

56.47 An ASIC EDA Flow for the Analysis and Prevention of DPA Side-Channel Attacks

Troy Hicks - *Revere Security, Addison, TX*
Jennifer Dworak - *Southern Methodist Univ., Dallas, TX*
Elif Alpaslan - *Advanced Micro Devices, Inc., Sunnyvale, CA*

56.48 Post-Silicon Bug Diagnosis with Inconsistent Executions

Andrew DeOrio, Daya Khudia, Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

56.49 Reverse Coverage Analysis

Avi Ziv, Ariel Birnbuam, Laurent Fournier, Steve Mittermaier - *IBM Corp., Poughkeepsie, NY*

56.50 FORMLESS: Scalable Utilization of Embedded Manycores in Streaming Applications

Matin Hashemi, Soheil Ghiasi - *Univ. of California, Davis, CA*

56.51 Power Aware Pfair Scheduling in Multiprocessor Real Time Systems

Nikhil Gupta and Suman Kaylan Mandal - Texas A&M Univ., Bryan, TX
Rabi Mahapatra - Texas A&M Univ., College Station, TX

COLOCATED EVENTS

In addition to DAC's full technical program, there are other conferences hosting their events at DAC. There is a separate registration fee to attend these meetings. If you are attending one of the conferences below, your registration does include entrance to the DAC Exhibit Hall Monday-Wednesday. Please note that a DAC Conference Registration does not include the colocated events.

Friday, June 3 12:00 - 6:00pm
Saturday, June 4 8:00am - 6:00pm
Sunday, June 5 8:00am - 12:00pm

Synthesis and FPGA **Univ. of California at San Diego**

INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS (IWLS)

Organizer(s):
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*
Igor Markov - *Univ. of Michigan, Ann Arbor, MI*
Philip Brisk - *Univ. of California, Riverside, CA*
Janet Wang- Univ. of Arizona, Tucson, AZ

The International Workshop on Logic and Synthesis is dedicated to research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers as well as abstracts highlighting important new problems in the early stages of development. The emphasis is on novelty and intellectual rigor.

Sunday, June 5 - Monday, June 6 8:00am - 6:00pm **General Interest** **Room: 30DE**

SIGDA DESIGN AUTOMATION SUMMER SCHOOL

Organizer(s):
Iris Bahar - *Brown Univ., Providence, RI*
Natasa Miskov-Zivanov - *Univ. of Pittsburgh, Pittsburgh, PA*
Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*

The Design Automation Summer School (DASS) offers graduate students the opportunity to participate in a two-day intensive course on selected areas of research and development in design automation (DA). Each topic of instruction in this course is covered by a distinguished speaker who defines the topic, describes recent accomplishments in considerable detail, and outlines upcoming challenges. Interactive discussions and follow-up activities among the participants round off an intensive, yet comprehensive activity geared towards graduate students in DA.

Sunday, June 5 - Monday, June 6 8:00am - 6:00pm **General Interest** **Room: 31AB**

IEEE INTERNATIONAL SYMPOSIUM ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST 2011)

General Chair: Ken Mai - *Carnegie Mellon Univ., Pittsburgh, PA*

Program Chair: Patrick Schaumont - *Virginia Polytechnic Institute and State Univ., Blacksburgh, VA*

Publicity Chair: Farinaz Koushanfar - *Rice Univ., Houston, TX*

A wide range of applications, from secure RFID tagging to high-end trusted computing, rely on dedicated and trusted hardware platforms. The security and trustworthiness of such hardware designs are critical to their successful deployment and operation. Recent advances in tampering and reverse engineering show that important challenges lie ahead. For example, secure electronic designs may be affected by malicious circuits - Trojans that alter system operation. Furthermore, dedicated, secure hardware implementations are susceptible to novel forms of attack that exploit side-channel leakage and faults. Third, the globalized, horizontal semiconductor business model raises concerns of trust and intellectual property protection. The IEEE International Symposium on Hardware Oriented Security and Trust is a forum for novel solutions to address these challenges. Innovative test mechanisms may reveal Trojans in a design before they are able to do harm. Implementation attacks may be thwarted using side-channel resistant design or fault-tolerant designs. New security-aware design tools can assist a designer in implementing critical and trusted functionality quickly and efficiently.

COLOCATED EVENTS

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Sunday, June 5 8:30am - 6:30pm **System-Level Design** **Room: 32AB**

SYSTEM-LEVEL INTERCONNECT PREDICTION (SLIP)

General Chair: Janet Wang - *Univ. of Arizona, Tuscon, AZ*
Program Chair: Deming Chen - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Finance Chair: Mustafa Ozdal - *Intel Corp., Hillsboro, OR*
Publicity Chair: Rasit Topaloglu - *GLOBALFOUNDRIES, Milpitas, CA*

Speaker(s):
Riko Radojcic - *Qualcomm, Inc., San Diego, CA*
Luca Benini - *Univ. di Bologna, Bologna, Italy*
Bob Patti - *Tezzaron Semiconductor, Naperville, IL*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*
Chuck Alpert - *IBM Corp., Austin, TX*

The 2011 System-Level Interconnect Prediction (SLIP) workshop will be colocated with the 48th IEEE/ACM Design Automation Conference on June 5, 2011 at the Convention Center, San Diego, CA. The general technical scope of the workshop is the design, analysis, and prediction of intercommunication fabrics in electronic systems. The organizing committee invites original contributions to the workshop. These contributions include papers, tutorials, panels, and special sessions. Regular papers will be double blind reviewed. We accept papers based on novelty and contributions.

Representative technical topics include, but are not limited to:

1. Interconnect prediction at various IC design stages
2. Interconnect design challenges and system-level NOC design
3. Design and analysis of power and clock networks
4. Interconnect architecture of structural designs and FPGAs
5. Interconnect fabrics of manycore architectures
6. Design For Manufacturing (DFM) techniques for interconnects
7. High speed PCB interconnect design
8. Design and analysis of chip-package interfaces
9. Interconnect topologies of multiprocessor systems
10. Interconnect design and prediction of through-silicon vias (TSV) in 3-D ICs
11. Emerging interconnect technologies, e.g., RF interconnects, photonic networks, and carbon-based interconnects.
12. Synergies between chip intercommunication networks and networks arising in other contexts such as social networks and system biology

Sunday, June 5 1:00 - 5:30pm
Monday, June 6 9:00am - 6:00pm **System-Level Design** **Room: 25C**

9TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS (SASP 2011)

General Co-Chair: Walid Najjar - *Univ. of California, Riverside, CA*
General Co-Chair: Georgi N. Gaydadjiev - *Delft Univ. of Technology, Delft, The Netherlands*
Technical Program Co-Chair: Philip Brisk - *Univ. of California, Riverside, CA*
Technical Program Co-Chair: Sami Yehia - *Thales Group, Paris, France*

The market for embedded processors is driven primarily by two factors: cost and volume. This has forced a reevaluation of the best way to satisfy users' needs for high performance and low-energy consumption without drastically increasing the complexity of the design process. Domain-specific embedded processors in markets such as network processing, automotive, and others, have splintered a pre-existing market for general-purpose, low-cost, low-energy processors. Reprogrammable and reconfigurable embedded processors, in contrast, offer a single, fixed-silicon device that could amortize manufacturing costs for low-to-medium volume market segments. SASP explores (micro)architectural design approaches, trade-offs, and compiler technologies, for both domain-specific and customizable embedded processors. The symposium is a forum wherein challenges and solutions will be explored, discussed, and compared.

Monday, June 6 - Tuesday, June 7 8:30am - 6:30pm
Wednesday, June 8 - Thursday, June 9 9:00am - 5:00pm **Emerging Technologies** **Room: 28CD**

NASA/ESA ADAPTIVE HARDWARE AND SYSTEMS (AHS)

Chair(s):
David Merodio Codinachs - *European Space Agency, Noordwijk, The Netherlands*

Organizer(s):
Tughrul Arslan - *Univ. of Edinburgh, Edinburgh, United Kingdom*
Umeshkumar Patel - *Goddard Space Flight Center, Greenbelt, MD*
Didier Keymeulen - *Jet Propulsion Laboratory, Pasadena, CA*

The purpose of the NASA/ESA Adaptive Hardware and Systems (AHS) conference is to bring together leading researchers from the adaptive hardware and systems community to exchange experiences and share new ideas in the field.

Adaptation reflects the capability of a system to maintain or improve its performance in the context of internal or external changes, such as uncertainties and variations during fabrication, faults and degradations, modifications in the operational environment, incidental or intentional interference, different users and preferences, modifications of standards and requirements, and trade-offs between performance and resources.

Adaptation at hardware levels increases the system capabilities beyond what is possible with software-only solutions, and a large number of adaptation features employing both analog and digital adjustments are becoming increasingly present in the most elementary system components. Algorithms, techniques, and their implementation in hardware are developed over a diverse variety of applications such as adaptive communications (adapting to changing environment and interferences), reconfigurable systems on a chip, and portable wireless devices (adapting to power limitations) or survivable spacecraft (adapting to extreme environments and mission unknowns). This meeting will provide a forum for discussion on the generic techniques of adaptive hardware and systems, with a focus on communications and space applications; with view to its expansion and exploitation in other applications such as consumer, medical, defense, and security.

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Monday, June 6 8:30am - 7:00pm **DFM and the Manufacturing Interface** **Room: 20D**

IEEE DESIGN FOR MANUFACTURING AND YIELD (DFM&Y) WORKSHOP

Organizer(s):
Rob Aitken - *ARM, Inc., San Jose, CA*
Puneet Gupta - *Univ. of California, Los Angeles, CA*

Increased manufacturing challenges in today's nanometer technologies require up-to-date solutions for yield optimization. Designing an SOC for manufacturability and yield aims at improving the manufacturing process, and consequently, its yield, by enhancing communications across the design-manufacturing interface. A wide range of Design for Manufacturability (DFM) and Design for Yield (DFY) methodologies and tools are in use today. Some of these are applied during the back-end design stages, including mask design, while others involve post design activities, from lithography through wafer sort, packaging, final test, and failure analysis.

DFM can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using a DFM solution is an investment and thus choosing the most cost effective one(s) requires trade-off analysis. The workshop analyzes the key trends and challenges in DFM and DFY, and provides an opportunity to discuss a range of DFM and DFY solutions for SOC designs now and in the future.

Monday, June 6 8:30am - 12:30pm **DFM and the Manufacturing Interface** **Room: 29AB**

SYNERGIES IN IC DESIGN: PDK AND DFM STANDARDS WORKING TOGETHER

Program Chair(s):
Jake Buurma - *Si2, San Jose, CA*
Nick English - *Si2, Austin, TX*
Bill Bayer - *Si2, Austin, TX*

Chair(s):
Sumit DasGupta - *Si2, Austin, TX*

Speaker(s):
Joe Mastroianni - *Mentor Graphics Corp., San Jose, CA*
Flavien DeLauche - *STMicroelectronics, Crolles, France*
Barry Nelson - *Cadence Design Systems, Inc., San Jose, CA*
Fred Valente - *Texas Instruments, Inc., Richardson, TX*
Bob Sayah - *IBM Corp., Hopewell Junction, NY*
Concetta Riccobene - *LSI Corp., San Jose, CA*

The complexity of rules and processes needed to ensure the manufacturability of ICs is increasing rapidly with every new technology node. Many of the issues involving Process Design Kits (PDKs) and Design for Manufacturability (DFM) are interrelated and can be simplified, if not eliminated, by standardized industry practices. This workshop will highlight those interrelated standards and showcase the ongoing work being done by industry leaders in solving these problems.

PDKs are the fundamental building blocks for all electronic design. Standardized representation of PDK content and interfaces will offer operating efficiencies to foundries, EDA companies, IP providers, and design companies who use the PDKs, create their own kits or need to modify those that they receive from their foundries. Resultant PDKs are expected to be more robust and portable than ever before.

In the DFM arena, standardization has proceeded along two parallel fronts. In physical DFM, a standard high-level DFM verification and optimization language called OpenDFM has been defined to support the needs of manufacturability and PDK generation. OpenDFM rules bridge the gap between a layout style that allows only a few, very restricted layout patterns and a style that allows purely arbitrary layouts. Second, there is ongoing effort to standardize a common format for representing parasitic information and to better handle manufacturing variability. This has implications in how this data is represented in PDKs and how they affect the modeling of design parameters for power, timing, and SI analysis.

Monday, June 6 1:00 - 4:30pm **Physical Design** **Room: 29AB**

OPENACCESS SCRIPTING LANGUAGE WORKSHOP

Program Chair: Nick English - *Si2, Austin, TX*
Publicity Chair: Bill Bayer - *Si2, Austin, TX*

Chair(s):
Sumit DasGupta - *Si2, Austin, TX*

Organizer(s):
Bill Bayer - *Si2, Austin, TX*

Speaker(s):
Rudy Albachten - *Advanced Micro Devices, Inc., Austin, TX*
Stefan Zager - *Advanced Micro Devices, Inc., Sunnyvale, CA*
James Masters - *Intel Corp., Folsom, CA*
John McGehee - *Voom, Inc., Los Altos, CA*

(NOTE: There will be a "Woz Pause" from 1:50PM - 3:10PM to allow attendees to see Steve Wozniak's Keynote from 2PM-3PM)

This tutorial is intended for chip design engineers who want to interact with OpenAccess programs or data in scripting languages (such as Tcl, Perl, Python, Ruby), either integrated with native C++ code or as stand-alone programs. These engineers use scripting languages as part of their daily work. This tutorial will provide them with an invaluable knowledge base of what is available to them today.

This tutorial will teach engineers the following key points:

1. How to use these API's in writing scripts to:
   Manage a design process/sub-process
   Create quick tools for custom functions with minimal performance degradation
   Create tools to perform "what if" evaluations as part of a design effort
2. The architecture of the OpenAccess Scripting (OAS) interfaces for four popular scripting languages:
   Perl - a procedural, syntax-rich language used for fast prototyping
   Tcl - a simple, command-based syntax used since 1993, supporting events, multiple interpreters, and OS-level threading
   Python - a mostly object-oriented language with garbage collection, operator overloading, reflection, free functions, closures, lists, iterators, and list comprehensions
   Ruby - an object-oriented language with garbage collection, operator overloading, reflection, access control, closures, and blocks
3. Procedures to
   Download the OAS package
   Install and build an OAS interfaces in the user's environment
4. Use of the OAS interfaces with detailed programming examples from the scripting language versions of the C++ Labs inthe Si2 OpenAccess API Tutorial

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Tuesday, June 7 - Wednesday, June 8 2:00 - 4:00pm **General Interest** **Room: 23C**

ACM STUDENT RESEARCH COMPETITION AT DESIGN AUTOMATION CONFERENCE

Organizer(s):
Naehyuck Chang - *Seoul National Univ., Seoul, Republic of Korea*
Srinivas Katkoori - *Univ. of South Florida, Tampa, FL*

The ACM Student Research Competition (SRC), sponsored by Microsoft Research, offers a unique forum for undergraduate and graduate students to present their original research before a panel of judges and attendees.

There are three rounds of competition and a grand finals competition:

1. Initial Selection – extended abstracts are reviewed and selected to present at DAC;
2. Poster Session (June 7th): Judges will review the posters and speak to participants about their research; a group of semi-finalists will be chosen for oral presentation;
3. Oral Presentation (June 8th): Semi-finalists will give a short presentation of their research before a panel of judges. Three winners will be chosen for each category undergraduate and graduate, receiving $500, $300, and $200 respectively.

The SRC Grand Finals (June 2012): All undergraduate and graduate student winners from this competition will advance to the SRC Grand Finals. A different panel of judges evaluates these winners against each other via the web. Three undergraduates and three graduates will be chosen as the SRC Grand Finals winners. They are invited, along with their advisors, to the annual ACM Awards Banquet (June 2012), where they receive formal recognition.

Important dates:

- Abstract submission deadline: April 8, 2011
- Acceptance notification: May 1, 2011
- Poster session at DAC: June 7, 2011
- Presentation session at DAC: June 8, 2011
- Award winners announced at DAC: June 9, 2011
- Grand Finals winners honored at ACM Awards Banquet: June 2012

This poster session is in conjunction with SIGDA member meeting and the Ph.D Forum.

Wednesday, June 8 - Thursday, June 9 8:00am - 5:30pm **Emerging Technologies** **Room: 28AB**

IEEE/ACM INTERNATIONAL SYMPOSIUM ON NANOSCALE ARCHITECTURES (NANOARCH '11)

Chair(s):
Csaba Andras Moritz - *Univ. of Massachusetts, Amherst, MA*

Organizer(s):
Ian O'Connor - *École Centrale de Lyon, Lyon, France*
Kang Wang - *Univ. of California, Los Angeles, CA*

NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS nanocomputing directions. The symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century - how to design, fabricate, and integrate nanosystems to overcome the fundamental limitations of CMOS. In particular, such systems could: (1) contain unconventional nanodevices with unique capabilities, including directions beyond simple switches, (2) introduce new logic and memory concepts, (3) involve novel circuit styles, (4) introduce new concepts for computing, (5) reconfigure and/or mask faults at much higher rates than in CMOS, (6) involve new paradigms for manufacturing, and (7) rethink the methodologies and design tools involved.

This seventh symposium introduces, for the first time, several new exciting sessions and opportunities for interaction. In addition to Regular papers presenting original techniques/directions, it invites the community to also submit Nanofabric Progress Updates giving a progress update of their nanofabrics directions to date across devices, circuits, architecture, and manufacturability aspects - e.g. 2-D/3-D nanowire, magnonic, memristor, CNT, graphene, FinFETs, and QCA based directions. In addition, Crosscut papers are invited from the broader nanotechnology community to highlight promising nanomaterial, nanodevice, nanomanufacturing, and integration ideas with application potential in nanoscale architectures.

Wednesday, June 8 - Thursday, June 9 10:00am - 6:00pm **General Interest** **Room: 26AB**

CELUG/EDA CONSORTIUM COLOCATED EVENT

Chair(s):
Lee Levenson - *CELUG, Tarzana, CA*
Paul Cohen - *EDA Consortium, Boston, MA*

EDA Licensing providers, ISVs, EDA/HPC IT Vendors, and users will come together at an event colocated with the Design Automation Conference in San Diego, June 8 and 9, 2011. CELUG (Centralized Enterprise Licensing Users Group) and EDAC (EDA Consortium) are co-hosting this two-day event at DAC 2011. This interactive event will focus on Enterprise Licensing and EDA/HPC IT, with presentations and panels addressing current and future challenges to making high-technology tools and users more productive.

This colocated event will bring together Licensing Solution Providers, Independent Software Vendors, and EDA/HPC IT Grid/Cloud/Infrastructure/Server/Storage Solution Companies face to face for interactive sessions with Enterprise Customers from key fields including:

Academia
Aerospace
Automotive
Oil and Gas
Semiconductor
Life Sciences
Chemical Analysis
Electronic Test
Electronic Measurement

PAVILION PANELS

EXHIBIT HALL D, BOOTH #3421

Sponsored by:

GLOBALFOUNDRIES

Monday, June 6 9:15 - 10:15am | **General Interest** | **Exhibit Hall D, Booth #3421**

GARY SMITH ON EDA: TRENDS AND WHAT'S HOT AT DAC

Chair(s):
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

Organizer(s):
Robert Gardner - *EDA Consortium, San Jose, CA*

Speaker(s):
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

Gary Smith of Gary Smith EDA reviews EDA's hottest technology trends. How will the dramatic changes in EDA, the semiconductor market, and the design community affect you? What are the hot 'must sees' at this year's conference? Find out here!

Monday, June 6 10:30 - 11:15am | **Emerging Technologies** | **Exhibit Hall D, Booth #3421**

3-D IC: MYTH OR MIRACLE?

Moderator(s):
Herb Reiter - *GSA Consultant for the 3-D IC Programs, Los Altos, CA*

Organizer(s):
Mike Santarini - *Xilinx, Inc., San Jose, CA*

Speaker(s):
Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
Riko Radojcic - *Qualcomm, Inc., San Diego, CA*
Suk Lee - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

Fewer companies can justify the costs of building ASICs and ASSPs in leading-edge process technologies. Many companies are considering implementing their next designs in 3-D technologies instead of monolithic die. What are the tool, methodology, and infrastructure challenges of 3-D IC design and what is needed to make stacked die devices mainstream?

Monday, June 6 11:30am - 12:15pm | **System-Level Design** | **Exhibit Hall D, Booth #3421**

HIGH-LEVEL SYNTHESIS: WHAT WORKS?

Moderator(s):
Gabe Moretti - *Gabe on EDA, Venice, FL*

Organizer(s):
Brett Cline - *Forte Design Systems, San Jose, CA*

Speaker(s):
Steve Frank - *Paneve, LLC, Hadley, MA*
Srikanth Muroor - *Telegent Systems, Inc., Sunnyvale, CA*
Olivier Schneider - *ST-Ericsson, Grenoble, France*

Join the experts as they debate strengths and weaknesses of today's high-level synthesis (HLS) tools as well as their approaches to implementing a high-level design flow customized to their needs. See how the experts incorporate HLS into their standard design flow, including system integration, synthesis, and verification.

Monday, June 6 3:30 - 4:30pm | **General Interest** | **Exhibit Hall D, Booth #3421**

WWED EVENT: CAREER VELOCITY VECTORS: THE EXCITEMENT OF ENGINEERING

Moderator(s):
Holly Stump - *Chair, Women in Electronic Design, Mountain View, CA*

Organizer(s):
Karen Bartleson - *Synopsys, Inc., Mountain View, CA*

Speaker(s):
Debi Coleman - *SmartForest Ventures, LLC, Portland, OR*
Limor Fix - *Intel Corp., Hillsboro, OR*
Christine King - *SMSC, Hauppauge, NY*

Engineering is still one of the most exciting careers today; it has transformed the world. Learn how you can develop your career for intellectual, personal, and business success. Panelists will describe velocity vectors: early career to the pinnacles of success, transitioning between academia and commercial enterprise, and how to be a star on your chosen path - technical or business.

Event Sponsor:

eve

PAVILION PANELS

EXHIBIT HALL D, BOOTH #3421

Sponsored by:

GLOBALFOUNDRIES

Monday, June 6 4:30 - 5:30pm | **General Interest** | **Exhibit Hall D, Booth #3421**

WORDS OF WISDOM: A CONVERSATION WITH THE MARIE R. PISTILLI AWARD WINNER

Moderator(s):
Peggy Aycinena - *EDA Confidential, San Mateo, CA*

Organizer(s):
Peggy Aycinena - *EDA Confidential, San Mateo, CA*

Join us for the presentation of the 12th annual Marie R. Pistilli Women in Electronic Design Automation (EDA) Achievement Award. The award honors leadership, and personal and professional contributions to women in the industry. An interview by Peggy Aycinena with Limor Fix, the 2011 Marie R. Pistilli Award winner, will follow.

Tuesday, June 7 11:00am - 12:00pm | **Business** | **Exhibit Hall D, Booth #3421**

HOGAN'S HEROES: THE REAGGREGATION OF ECOSYSTEM VALUE

Moderator(s):
Jim Hogan - *Tela Innovation, Inc., Campbell, CA*

Organizer(s):
Daniel Nenni - *SemiWiki, Danville, CA*

Speaker(s):
Ajoy K. Bose - *Atrenta, Inc., San Jose, CA*
Jack Harding - *eSilicon Corp., Sunnyvale, CA*
Grant A. Pierce - *Sonics, Inc., Milpitas, CA*

The semiconductor ecosystem shifts its value aggregation on somewhat predictable cycles. These are followed by longer periods of stability during which new companies are created. The latest cycle is being driven by system houses. What impact will these new trends in system design have on EDA and IP business models and enterprise value?

Tuesday, June 7 1:00 - 1:45pm | **Synthesis and FPGA** | **Exhibit Hall D, Booth #3421**

C-TO-FPGA TOOLS: READY FOR THE MASS MARKET?

Moderator(s):
Kevin Morris - *Techfocus Media, Inc., Portland, OR*

Organizer(s):
Mike Santarini - *Xilinx, Inc., San Jose, CA*

Speaker(s):
Jeff Bier - *Berkeley Design Technology, Inc., Oakland, CA*
Simon Bloch - *Mentor Graphics Corp., Wilsonville, OR*
Johannes Stahl - *Synopsys, Inc., Mountain View, CA*

FPGAs are no longer just used by logic designers. Embedded designers and algorithm developers place FPGAs at the heart of their designs. For FPGA vendors to capitalize on the market, viable C-to-FPGA tools are required. Is the current batch of tools up to the task? What are the FPGA and EDA vendors doing to serve this broad user base?

Tuesday, June 7 2:00 - 2:45pm | **Verification and Test** | **Exhibit Hall D, Booth #3421**

VERIFICATION: WHAT'S IN YOUR WALLET?

Moderator(s):
John Blyler - *Chip Design Magazine, San Francisco, CA*

Organizer(s):
David Park - *Synopsys, Inc., Hillsboro, OR*

Speaker(s):
John Goodenough - *ARM, Ltd., San Jose, CA*
Scott Runner - *Qualcomm, Inc., San Diego, CA*
Jim Miller - *Advanced Micro Devices, Inc., San Jose, CA*

Verification continues to devour over 70% of an ever-shrinking project cycle, and the ITRS roadmap predicts that this horror will only increase. Executive panelists, whose companies' success depends on fast and comprehensive verification, will describe their verification methodologies, what technologies they are betting on looking forward, and how they use ROI as a criterion for the verification tools they evaluate.

PAVILION PANELS

EXHIBIT HALL D, BOOTH #3421

Sponsored by:

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Tuesday, June 7 3:00 - 3:45pm | **Emerging Technologies** | **Exhibit Hall D, Booth #3421**

3-D EXTRACTION: COMING TO A DESIGN NEAR YOU?

Moderator(s):
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

Organizer(s):
Daniel Payne - *Marketing EDA, Tualatin, OR*

Speaker(s):
Carey Robertson - *Mentor Graphics Corp., Wilsonville, OR*
Ji Zheng - *Apache Design Solutions, Inc., San Jose, CA*
Kaladhar Radhakrishnan - *Intel Corp., Phoenix, AZ*

Smaller IC geometries and higher switching speeds require more accurate modeling and simulation technologies. Traditional pattern-based matching and rule-based extraction methods may not be accurate enough for today's IC and package designs. 3-D extraction tool providers and designers will discuss 3-D field solver technology requirements, applications, and benefits.

Tuesday, June 7 4:00 - 4:45pm | **Embedded Systems and Software** | **Exhibit Hall D, Booth #3421**

MULTICORE: MADNESS OR JUST TODAY'S CHAOS?

Moderator(s):
Grant Martin - *Tensilica, Inc., Santa Clara, CA*

Organizer(s):
Andrea Kroll - *Huawei Technologies Co., Ltd., San Jose, CA*

Speaker(s):
Drew Wingard - *Sonics, Inc., Milpitas, CA*
Paul Tobin - *Advanced Micro Devices, Inc., Boxboro, MA*
Debashis Bhattacharya - *Huawei Technologies Co., Ltd., Plano, TX*

Multicore SOCs are commonplace; driven by the need for higher performance, lower price, and power-efficient solutions. This panel will discuss the challenges in selecting and integrating IP, interconnect performance, and embedded software and tools, as well as key requirements for building a successful SOC.

Tuesday, June 7 5:00 - 5:45pm | **Embedded Systems and Software** | **Exhibit Hall D, Booth #3421**

ANDROID, MEEGO, AND LINUX: WHERE IS IT ALL HEADING?

Moderator(s):
Jim Zemlin - *Linux Foundation, San Francisco, CA*

Organizer(s):
Andrea Kroll - *Huawei Technologies Co., Ltd., San Jose, CA*

Speaker(s):
Gerard Andrews - *Texas Instruments, Inc., Stafford, TX*
Simon Davidmann - *Imperas Software Limited, Oxfordshire, United Kingdom*
Eric Dewannain - *Tensilica, Inc., Santa Clara, CA*

Android, MeeGo, Embedded Linux, Windows Mobile, Chrome, Symbian, iOS... What are the business and technical opportunities and challenges in supporting these open source and proprietary operating systems? What is required to stay ahead in the industry? For hardware providers? For embedded software developers?

Wednesday, June 8 9:15 - 10:15am | **Business** | **Exhibit Hall D, Booth #3421**

TOWN HALL: WHAT EDA ISN'T DOING RIGHT

Moderator(s):
Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*

Organizer(s):
Mike Santarini - *Xilinx, Inc., San Jose, CA*

Speaker(s):
Behrooz Abdi - *NetLogic Microsystems, Inc., Santa Clara, CA*
Charles Matar - *Qualcomm, Inc., San Diego, CA*
Alan Nakamoto - *PMC-Sierra, Inc., Burnaby, BC, Canada*

The EDA industry has suffered through a bit of a malaise in recent years in terms of startup innovation, M & A activities, and public visibility. Lucio and his panel of tool and IP users will examine what the EDA industry could do to better serve customers and move to a brighter future.

PAVILION PANELS

EXHIBIT HALL D, BOOTH #3421

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Wednesday, June 8 10:30 - 11:15am | **Analog/Mixed-Signal/RF Design** | **Exhibit Hall D, Booth #3421**

WHY THE DELAY IN ANALOG PDK?

Moderator(s):
Steven Klass - *SMSC, Phoenix, AZ*

Organizer(s):
Daniel Nenni - *SemiWiki, Danville, CA*

Speaker(s):
Mass Sivilotti - *Tanner EDA, Monrovia, CA*
Tom Quan - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Ofer Tamir - *TowerJazz, Newport Beach, CA*

Why does it take so long for foundries to release analog/mixed-signal process design kits (PDKs)? The amount of AMS content in your designs is growing, and the pressure to move to smaller process nodes is increasing. This is your chance to talk to the people who develop your PDKs and reference flows!

Wednesday, June 8 1:00 - 1:45pm | **Business** | **Exhibit Hall D, Booth #3421**

STOP THAT THIEF! - IP IN GLOBAL MARKETS

Moderator(s):
Adam Traidman - *Cadence Design Systems, Inc., San Jose, CA*

Organizer(s):
Ron Moore - *ARM, Ltd., San Jose, CA*

Speaker(s):
Gerd Teepe - *GLOBALFOUNDRIES, Dresden, Germany*
Alan Coady - *Integrated Device Technology, Inc., Ottawa, ON, Canada*
Jonathan T. Kaplan - *Law Office of Jonathan T. Kaplan, Vancouver, WA*

IP reuse is the de-facto model for SOC development. Emerging markets are increasingly becoming both consumers and suppliers of design IP. Panelists involved in the development and integration of IP discuss the technical, business, and legal aspects of cross-regional IP sourcing. What can the IP ecosystem do to promote business integrity worldwide?

Wednesday, June 8 2:00 - 2:45pm | **General Interest** | **Exhibit Hall D, Booth #3421**

TEENS TALK TECH: YOU DON'T KNOW JACK

Moderator(s):
Karen Bartleson - *Synopsys, Inc., Mountain View, CA*

Organizer(s):
Yatin Trivedi - *Synopsys, Inc., Mountain View, CA*

Speaker(s):
Andrew Ng - *Rancho Bernardo High School, San Diego, CA*
Scarlett Chen - *Rancho Bernardo High School, San Diego, CA*
Aria Fariborzi - *Rancho Bernardo High School, San Diego, CA*

High school students tell us how they use the latest tech gadgets, and what they expect to be using in three to five years. They give insights into the next killer applications and what they would like to see in the next generation of hot, new electronics products that we should be designing now.

Wednesday, June 8 3:00 - 3:45pm | **Low-Power Design** | **Exhibit Hall D, Booth #3421**

LOW-POWER REPORT CARD: ARE WE COOL?

Moderator(s):
Ed Sperling - *Low Power Engineering, San Jose, CA*

Organizer(s):
Yukari Ohno - *Apache Design Solutions, Inc., San Jose, CA*

Speaker(s):
Ambrose Low - *Broadcom Corp., San Jose, CA*
Ruggero Castagnetti - *LSI Corp., Milpitas, CA*
Andrew Brotman - *GLOBALFOUNDRIES, Milpitas, CA*

Low-power design has been the "hot" topic for several years. Designers have tried to meet power budget requirements using a multitude of methods, including algorithmic optimizations, circuit design techniques, manufacturing processes, and EDA tool offerings. But are we really more energy-efficient today? This panel will assess which methods have produced the best results.

PAVILION PANELS

EXHIBIT HALL D, BOOTH #3421

Sponsored by:

GLOBALFOUNDRIES

Wednesday, June 8 4:00 - 4:45pm | **Synthesis and FPGA** | **Exhibit Hall D, Booth #3421**

IP AND FPGAS: WHERE'S MY FREE LUNCH?

Moderator(s):
Gabriele Saucier - *Design and Reuse, Grenoble, France*

Organizer(s):
Yervant Zorian - *Synopsys, Inc., Mountain View, CA*

Speaker(s):
Rick Tomihiro - *Xilinx, Inc., San Jose, CA*
Hal Barbour - *CAST, Inc., Woodcliff Lake, NJ*
Kurt Shuler - *Arteris, Inc., Sunnyvale, CA*

In the past, IP was considered as a free add-on to FPGA packages. With today's complex FPGA-based designs, IP blocks are growing in strategic importance. To speed up the design process, FPGA and third-party vendors offer comprehensive IP portfolios. Where is the real meat in the FPGA market? Panelists discuss how IP stimulates innovation and drives new business models.

Wednesday, June 8 5:00 - 5:45pm | **General Interest** | **Exhibit Hall D, Booth #3421**

PISTILLI'S PERSPECTIVE: EDA FUTURE - FEAST OR FAMINE

Moderator(s):
Thomas Pennino - *TP Technologies, LLC, Holmdel, NJ*

Organizer(s):
Ron Moore - *ARM, Ltd., San Jose, CA*

Speaker(s):
Pat Pistilli - *MP Associates, Inc., Louisville, CO*

For almost 50 years, the EDA industry has bridged the productivity gap with every new process node adoption. Join Thomas Pennino, former Bell Labs Director and past DAC General Chair, for a discussion with Pat Pistilli, 2010 winner of the Phil Kaufman Award, on invention and reinvention of the EDA industry to meet the design challenges of the next half-century.

ADJUNCT EVENTS

Tuesday, June 7 12:00 - 2:00pm **General Interest** **Room: 25AB**

IEEE CEDA: THE TRUTHS AND MYTHS OF EMBEDDED COMPUTING

Organizer(s):
Dwight Hill - *Synopsys, Inc., Mountain View, CA*

Speaker(s):
Shekhar Borkar - *Intel Corp., Portland, OR*

Computers have become ubiquitous - from powerful data centers housing supercomputing clusters, to tiny microcontrollers in your toothbrush. However, the embedded computing discipline does not get its fair share of attention. In this talk, we will define the scope of embedded computing, compare it to general purpose computing with appropriate metrics, challenge the myths that float around, and uncover the truths.

We will discuss challenges in architecture, design, and test of future embedded computers, which will become omnipresent, even as part of the general purpose computers.

Tuesday, June 7 7:00 - 8:30pm **General Interest** **Room: 20D**

14TH ANNUAL SIGDA PH.D. FORUM/MEMBER MEETING

SIGDA invites you to attend our 14th annual Ph.D. Forum and Member Meeting at DAC 2011. SIGDA members are invited, as are all members of the EDA Community. We will begin with an overview of SIGDA programs, including newly created programs, followed by the presentation of this year's ACM/SIGDA Awards.

However, the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research and gives the EDA community a preview of work in progress. Light refreshments will be served.

ADDITIONAL MEETINGS

Monday, June 6 10:00 - 11:00am **Business** **Room: 24A**

SHOW ME THE MONEY

Jim Hogan and Paul McLellan present their views on how the value chain for the design and manufacture of electronic systems is changing, and where the money will be made in the future. In particular, what it means for EDA, IP, embedded software tool suppliers and SoC designers.

Monday, June 6 12:00 - 1:30pm **Analog/Mixed-Signal/RF Design** **San Diego Marriott, Marina Ballroom D-E**

INTEROPERABLE PDK STANDARDS ARE HERE TO STAY: NEW ERA OF ANALOG/CUSTOM INNOVATION

At the fifth annual IPL Luncheon, the IPL Alliance will present an update on the current and future success of IPL standards.

Attendees will hear about:

How the industry is embracing the IPL 1.0 standard
Specs of the new interoperable design constraint standard
Collaboration among standards: How oPDK and iPDK will work together

Monday, June 6 4:30 - 6:00pm **General Interest** **Room: 29AB**

ANNUAL SI2 OPEN RECEPTION

Organizer(s):
Bill Bayer - *Si2, Austin, TX*

This reception is free and open to all who are interested in Si2 activities such as OpenAccess, DFM, low-power design, 3D ICs, and OpenPDKs. The keynote speaker will be Philippe Magarshack, Group Vice-President - Central R&D, STMicroelectronics.

In celebration of over 23 years of service to the IC design industry, refreshments, and light hors d'oeuvres will be served.

Monday, June 6 6:00 - 7:00pm **General Interest** **Center Terrace**

MONDAY NIGHT COCKTAIL RECEPTION

Please join us outside on the Center Terrace for cocktails and networking.

Co-Sponsored by:

Apache ARM

Monday, June 6 6:00 - 8:00pm **Other** **San Diego Marriott Hotel, Marina Ballroom F**

PRIMETIME SPECIAL INTEREST GROUP (SIG) RECEPTION FEATURING NEXT GENERATION ECO GUIDANCE TECHNOLOGY

Synopsys hosts an annual dinner event for the PrimeTime Special Interest Group at DAC, providing an opportunity for PrimeTime users to stay connected with the latest developments in timing analysis. This year, the event will launch Synopsys' 3rd generation PrimeTime ECO guidance technology. Synopsys' R&D team will unveil the new underlying engines and industry experts will share their experience on this exciting new technology resulting in up to 10X faster and better quality of results with less ECO changes.

Monday, June 6 6:00 - 8:00pm **General Interest** **San Diego Marriott Hotel, Marina Ballroom D & E**

SYNOPSYS/DELL UNIVERSITY RECEPTION

University professors and students are invited to join Synopsys and Dell, in cooperation with MSE, for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

What Did We Really Learn from the Hubble Experience?
Kevin P. Thompson, Ph.D. - *Group Director, Research and Development, Synopsys*

Era of Customization and Implications to EDA
Jason Cong, Ph.D. - *Director, Center for Domain-Specific Computing, Chancellor's Professor, UCLA*

ADDITIONAL MEETINGS

Tuesday, June 7 7:15 - 8:45am **General Interest** **Marriott Hotel, Marquis North Ballroom F & G**

ARM –GLOBALFOUNDRIES - SAMSUNG - SYNOPSYS BREAKFAST

Join us for breakfast while industry experts from ARM, GLOBALFOUNDRIES, Samsung and Synopsys discuss our unique design enablement collaboration that delivers proven design, IP and manufacturing solutions for ARM-Powered® designs on the Common Platform Technology Alliance 32nm and 28nm high-k metal-gate (HKMG) process technologies.

Tuesday, June 7 6:00 - 7:00pm **General Interest** **Center Terrace**

TUESDAY NIGHT COCKTAIL RECEPTION

Please join us outside on the Center Terrace for cocktails and networking.

Sponsored by: ATRENTA

Tuesday, June 7 7:00 - 8:30pm **General Interest** **Room: 31C**

BIRDS-OF-A-FEATHER MEETING: GSA IP WORKING GROUP

Organizer(s):
Warren Savage - *IPextreme, Campbell, CA*

An informal meeting between the members of the Global Semiconductor Association's IP Working Group and interested parties from the semiconductor and EDA community to discuss the latest issues confronting the industry.

Tuesday, June 7 7:00 - 8:30pm **General Interest** **Room: 31AB**

BIRDS-OF-A-FEATHER MEETING: SOFT IP TAGGING STANDARDIZATION KICKOFF

Organizer(s):
Kathy Werner - *Freescale Semiconductor, Inc., Austin, TX*

Soft IP, particularly from third party vendors, must be tracked to satisfy contractual obligations such as royalty reporting and usage. Control of the third party IP source is lost once an IP is licensed, unlocked or otherwise made available in clear code.

This meeting will discuss the problem space and the opportunities to contribute in the new Accellera technical committee being formed to address the issues.

Wednesday, June 8 7:30 - 9:20am **Interconnect and Reliability** **San Diego Marriott Hotel, Marina Ballroom F**

SYNOPSYS INTEROPERABILITY BREAKFAST: ON SAFARI WITH CUSTOM DESIGN INTEROPERABILITY AND INTERCONNECT MODELING STANDARDS

Chi-Foon Chan, President and COO of Synopsys, invites you to attend Synopsys' interoperability breakfast sponsored by HP.

Hear the latest on the industry's collaborative efforts benefiting advanced custom design. See how the interconnect technology format is fostering greater efficiency in advanced node modeling and design.

Find out who wins the Tenzing Norgay Interoperability Achievement Award.

Wednesday, June 8 6:00 - 7:00pm **General Interest** **Sails Pavilion**

WEDNESDAY NIGHT COCKTAIL RECEPTION

Please join us in the Sails Pavilion for cocktails, networking and the Work in Progress (WIP) poster presentations. There will be over 50 poster presentations with interesting ideas for discussion.

EXHIBITOR FORUM
EXHIBIT HALL G, BOOTH#1005

Monday, June 6 10:00 - 10:35am | **General Interest** | **Exhibit Hall G - Booth #1005**

UNIFIED DESIGN METHODOLOGY FOR ADVANCED MIXED-SIGNAL DESIGN
PRESENTED BY: CADENCE DESIGN SYSTEMS, INC.

Speaker(s):
Mladen Nizic - *Cadence Design Systems, Inc., San Jose, CA*

Traditional mixed-signal design methodologies develop analog and digital components in disjointed environments, leading to problems with data conversion and management, design intent communication, and project visibility across functional teams. Cadence will present a unified methodology for realizing mixed-signal designs that eliminates overdesign, speeds convergence, and reduces overall design costs. By tightly integrating analog/RF and digital content through the OpenAccess database, the Cadence mixed-signal design methodology enables cross-domain interoperability and facilitates collaboration among analog and digital designers on design, verification, implementation, and signoff to hit specification and schedule targets.

Monday, June 6 10:40 - 11:15am | **General Interest** | **Exhibit Hall G - Booth #1005**

ANALOG IC DESIGN - WHY A COHESIVE TOOL FLOW DRIVES PRODUCTIVITY
PRESENTED BY: TANNER EDA

Speaker(s):
John Zuk - *Tanner EDA, Monrovia, CA*
Mass Sivilotti - *Tanner EDA, Monrovia, CA*

As Analog IC Designers strive to keep pace with the rapidly increasing market demands around quicker time-to-market, productivity has become a mandate. This presentation will discuss the productivity advantages afforded by using a cohesive analog design tool suite; comprised of schematic capture, simulation, layout, and physical verification. Findings from a recent survey of Analog IC Designers - touching on the key benefits and challenges they see with using a full-flow design suite - will be presented and discussed.

Monday, June 6 11:20 - 11:55am | **General Interest** | **Exhibit Hall G - Booth #1005**

MAGMA DESIGN AUTOMATION:
PUTTING ANALOG & DIGITAL DESIGN INTO HIGH GEAR
PRESENTED BY: MAGMA DESIGN AUTOMATION, INC.

Speaker(s):
Behrooz Zahiri - *Magma Design Automation, Inc., San Jose, CA*

Virtually every SoC today combines digital and analog functions. Analog content is increasing and digital content is getting more complex. In this presentation, Magma will reveal innovative technologies that put digital and analog implementation flows into high gear, enabling designers to accelerate schedules and deliver the best products into competitive marketplaces. We'll explain how the Talus® FX digital implementation system automatically handles over 10 million cells flat. We'll also discuss how Titan™ shifts analog design from hand-crafted to highly automated through new optimization engines that take process-independent specifications and generate robust devices with SPICE-accurate results.

EXHIBITOR FORUM

EXHIBIT HALL G, BOOTH#1005

Monday, June 6 3:00 - 3:35pm | **Analog/Mixed-Signal/RF Design** | **Exhibit Hall G - Booth #1005**

ANALOG IC DESIGN AT THE EDGE: A NEW TWIST FOR NANOSCALE PRODUCTIVITY
PRESENTED BY: TANNER EDA

Speaker(s):
Dr. Lanny Lewyn - *Lewyn Consulting, Laguna Beach, CA*
Nicolas Williams - *Tanner EDA, Monrovia, CA*

Nanoscale analog IC design productivity is a major concern as chip device counts approach 1 billion at 32 nm. A multitude of physical device pattern separation dimensions must now be entered into the prelayout simulation models to accurately predict postlayout circuit performance. Our approach - based on the seminal work of Mead and Conway - offers a novel method that enables rapid circuit simulation in a multitude of nanoscale technology nodes and platform options. The result is that prelayout simulation accuracy is improved; having a direct impact on increasing analog IC manufacturing yields while simultaneously increasing design productivity.

Monday, June 6 3:40 - 4:15pm | **Analog/Mixed-Signal/RF Design** | **Exhibit Hall G - Booth #1005**

WINNING THE WAR: TRACKING DESIGN PROGRESS FROM SYNTHESIS TO CLOSURE
PRESENTED BY: TUSCANY DESIGN AUTOMATION, INC.

Speaker(s):
Matthew Michels - *Tuscany Design Automation, Inc., San Jose, CA*

Every chip is a battle; against complexity, time, and the unknown.

Tuscany's Pinpoint is the battle map, delivering instant visual summaries of the live action across the design flow for each block and the full chip.

Pinpoint brings clarity out of gigabytes of data, improving decisions, eliminating surprises, and accelerating progress. It enables global teams to collaborate over the web and share best practices.

Come see how customers are benefiting from Pinpoint and how simple it is to install and use.

Monday, June 6 4:20 - 4:55pm | **Analog/Mixed-Signal/RF Design** | **Exhibit Hall G - Booth #1005**

DESIGN OPTIMIZATION USING THE NANGATE DESIGN OPTIMIZER AND 28 NM MEGALIBRARY
PRESENTED BY: NANGATE, INC.

Speaker(s):
Jens C. Michelsen - *Nangate, Inc., Sunnyvale, CA*

This presentation describes a methodology for design optimization in deep-submicron technologies. Getting full mileage out of modern technology nodes is getting more difficult: Traditional standard cell-based approaches lead to inferior results, and full-custom techniques are prohibitively expensive.

The described approach is based on a MegaLibrary, an extended library containing upwards of 10,000 fine-grained cell variants. The MegaLibrary is complemented by the Design Optimizer, an optimization tool, which integrates seamlessly with existing design flows to take advantage of the rich libraries.

EXHIBITOR FORUM
EXHIBIT HALL G, BOOTH#1005

Tuesday, June 7 11:00 - 11:35am | **System-Level Design** | **Exhibit Hall G - Booth #1005**

FUNDAMENTALS OF FULL-CHIP SUBSTRATE NOISE ANALYSIS FLOW FOR MIXED-SIGNAL DESIGNS
PRESENTED BY: APACHE DESIGN SOLUTIONS, INC.

Speaker(s):
Karan Sahni - *Apache Design Solutions, Inc., Sunnyvale, CA*

High switching digital activity impacts the performance of noise sensitive analog circuit through its substrate, requiring analysis solution that can accurately quantify the origin and propagation of this noise. Apache's substrate noise analysis flow considers digital substrate noise signature, power/ground supply noise coupling, package/board parasitic impact, and switching scenario influence. Totem™, a full-chip substrate noise analysis solution enables noise propagation analysis driving floor-planning and isolation technique implementations as well as accurate final validation with substrate noise back-annotation for IP simulation.

Tuesday, June 7 1:00 - 1:35pm | **General Interest** | **Exhibit Hall G - Booth #1005**

SOLUTIONS FOR FULL-CHIP LEVEL AUTOMATED ELECTROSTATIC DISCHARGE (ESD) DESIGN AND VERIFICATION
PRESENTED BY: APACHE DESIGN SOLUTIONS, INC.

Speaker(s):
Karthik Srinivasan - *Apache Design Solutions, Inc., San Jose, CA*

Prevalence of flip-chip designs, technology scaling and higher device densities make today's SoCs increasingly susceptible to ESD failures, requiring design and verification solutions that help protect against HBM/MM and CDM events. Apache's PathFinder™, a full-chip layout-based ESD integrity solution can handle multi-million gate designs with mixed digital and analog content and many power/ground domains. PathFinder flow enables early ESD planning for optimal clamp placement and help identify regions that violate design rules and resolve current density and voltage drop issues.

Tuesday, June 7 1:40 - 2:15pm | **General Interest** | **Exhibit Hall G - Booth #1005**

DFM: STARTING WITH THE END IN MIND AND "IN-DESIGN"
PRESENTED BY: CADENCE DESIGN SYSTEMS, INC.

Speaker(s):
Manoj Chacko - *Cadence Design Systems, Inc., San Jose, CA*

Design for manufacturing (DFM) is a critical step in the advanced node design flow to safeguard physical integrity and parametric performance. In this presentation, you'll learn about in-design DFM technologies and methodologies that allow designers to perform block-, IP-, and SoC-level physical and electrical variability checks - at every stage in the design cycle - to predictably deliver the highest yielding silicon to the foundry. By maintaining design intent and leveraging new abstraction techniques, in-design DFM enables convergence on silicon realization goals.

EXHIBITOR FORUM

EXHIBIT HALL G, BOOTH#1005

Tuesday, June 7 2:20 - 2:55pm | **General Interest** | **Exhibit Hall G - Booth #1005**

GLOBALFOUNDRIES 28NM DIGITAL REFERENCE FLOWS: SIGN-OFF READY FLOWS OPTIMIZED FOR MANUFACTURABILITY AND DESIGN ROBUSTNESS
PRESNENTED BY: GLOBALFOUNDRIES

Speaker(s):
Steven Chan - *GLOBALFOUNDRIES, Milpitas, CA*

This talk describes how manufacturability and design robustness are addressed in GLOBALFOUNDRIES' 28nm digital reference flows. Using design studies, efficient implementation of recommended design rules and automatic fixing of lithographic hot-spots in digital routing will be described. Techniques and methodologies to increase robustness and reduce the marginality of designs at 28nm will also be presented.

Tuesday, June 7 3:00 - 3:35pm | **General Interest** | **Exhibit Hall G - Booth #1005**

ESSENTIALS FOR TIMING SIGN-OFF: GOLDTIME POCV / MXO / SI
PRESENTED BY: EXTREME DA CORP.

Speaker(s):
Ayhan Mutlu - *Extreme DA Corp., Santa Clara, CA*

Timing closure is getting a lot harder as designs move to 28nm, with longer turn-around-times and more analysis uncertainty. Higher capacity and faster sign-off solutions are necessary but not sufficient. Getting the most performance from the latest node requires using advanced techniques for timing sign-off and to deliver ECOs within the same sign-off environment. Advanced techniques such as Parametric-OCV, efficient MM/MC analysis, dynamic and static voltage scaling, and understanding the delay impact of simultaneous switching inputs will be covered.

EXHIBITOR FORUM
EXHIBIT HALL G, BOOTH#1005

Tuesday, June 7 3:40 - 4:15pm | **General Interest** | **Exhibit Hall G - Booth #1005**

RTL TO SILICON POWER INTEGRITY FLOW FOR EARLY WHAT-IF PROTOTYPING AND SIGN-OFF ANALYSIS OF THE POWER DISTRIBUTION NETWORK (PDN)
PRESENTED BY: APACHE DESIGN SOLUTIONS, INC.

Speaker(s):
Preeti Gupta - *Apache Design Solutions, Inc., San Jose, CA*

The SOC Power Delivery Network (PDN) design and verification is an increasingly challenging and critical problem. Complex power management strategies, multiple low power modes, and transitions thereof, further increase the complexity. The Apache 'RTL to Silicon Power Integrity Flow' utilizes data available during RTL design phase, versus guesstimates, to enable early PDN prototyping including package decisions. The flow additionally strengthens power integrity sign-off by utilizing RTL simulations to increase analysis coverage across power-critical switching scenarios, otherwise missed with current methodologies.

Tuesday, June 7 4:20 - 4:55pm | **General Interest** | **Exhibit Hall G - Booth #1005**

ARM, CADENCE AND TI EXPLAIN CACHE COHERENT DESIGN OPPORTUNITIES AND VERIFICATION CHALLENGES: ACTUAL EXPERIENCES WILL BE SHARED
PRESENTED BY: CADENCE DESIGN SYSTEMS, INC.

Speaker(s):
Paul Martin - *ARM, Ltd., Berkshire, United Kingdom*
Mirit Fromovich - *Cadence Design Systems, Inc., San Jose, CA*
Velayutham "Velu" Durairaj - *Texas Instruments, Inc., Dallas, TX*

The trend to employ multiple processors in mobile/internet devices (e.g., smartphones, tablets) is driving the need to design in and verify cache coherent SOCs/systems. ARM describes how the introduction of the AMBAÂ® 4 ACE protocol and Cortex-A15 processor have lowered design barriers. That said, coherency verification challenges are now greater than ever. Cadence and TI describe approaches for ensuring that coherency is maintained system-wide (i.e., only up to date data is used and deadlocks avoided) and discuss actual experiences doing so.