#62DAC

THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

AI

Systems

Security

Design

EDA

June 22 -25, 2025

Moscone Center West | San Francisco, CA

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DEAR COLLEAGUES,

Welcome to the **62nd DAC, the Chips to Systems Conference,** where we come together to **shape the next generation of electronics!**

We're thrilled to welcome you to San Francisco, California, one of the world's most beautiful cities and a global hub for high-tech innovation. For this week, San Francisco becomes the design and design automation capital of the world! There's so much for you across the three vibrant floors of the Moscone West Convention Center.

DAC is unique in bringing together industry and academic researchers, designers, developers, vendors, and training partners under one roof. It's the premier venue for both learning and networking — opportunities that go well beyond the technical sessions. Join us for evening networking and poster sessions on Sunday, Monday, and Tuesday. This year, we're also offering twice-daily coffee breaks on both the exhibition and research floors, along with snack bars to keep you energized throughout the day.

Now in its 62nd year, DAC continues to lead the world in design and design automation, spanning everything from chips to complete systems. This year, our five core themes—*Design, EDA, Systems, AI, and Security*—are closely aligned with key technology trends such as *Low Power, Chiplets, Cloud, and Security.* These themes also reflect pressing industrial needs like *Aerospace & Defense, Automotive, Consumer Electronics, Data Centers, and Industrial Systems.*

Thanks to the dedication of countless volunteers, the DAC Executive Committee has assembled a dynamic four-day program packed with top-tier research sessions, expert design forums, and a robust exhibition.

This year's DAC features three inspiring keynotes, offering perspectives from both industry and academia on semiconductors, AI, and EDA. You also won't want to miss our SKYtalks, TechTalks, and Analyst Reviews—covering cutting-edge technologies, systems, applications, and trends shaping the future.

Our Research Track showcases 420 accepted papers across 30 tracks, selected from a record-breaking 1,862 submissions — a 20% increase over last year. The program also includes seven Special Sessions featuring invited presentations from leading experts. Five Tutorials and six Workshops on Sunday will offer additional training and hands-on learning opportunities. Be sure to check out the Late-Breaking Results and Work-in-Progress poster sessions for a preview of emerging directions in the field.

Complementing this is the vibrant Engineering Track, tailored for chip designers and technical managers. With strong focus areas including Front-End design, Back-End design, IP, AI, Systems and Software, and Chiplets. This year's submissions reflect continued growth with over 5.8% increase from the previous year. The track also includes special sessions and panels led by prominent industry experts and executives.

As always, exhibit floor remains a hub of excitement, with over 120 exhibitors and 25 first-time exhibitors. There are three Pavilions to experience:

- **DAC Pavilion on Level 2** – Experience the very forefront of innovation.
- **Exhibitor Forum on Level 1** – Get first-hand information on new tools and methodologies.
- **EE Times Chiplet Pavilion on Level 2** – Explore sessions and exhibitors focused on the design and implementation of Chiplets.

For a quick bite to eat or a beverage, visit the **Grab 'n Go Concession Area at the back of the 1600 Aisle on Level 1.** And don't forget that DAC is hosting a **Career Development Day** for early career and student attendees on Tuesday from 10:00 AM – 3:30 PM just inside the Level 1 exhibit hall.

To ensure you don't miss a moment, download the DAC Mobile App — it's your best tool for planning your schedule, navigating all three levels of Moscone West, and staying updated throughout the week.

I look forward to seeing and speaking with many of you in San Francisco, June 22–25. Together, let's LEARN TODAY and CREATE TOMORROW.

Enjoy the DAC 62!

HELEN LI

62nd DAC General Chair

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CONFERENCE INFORMATION

Exhibit Hours

Location: First and Second Floor

Monday	10:00 AM – 6:00 PM
Tuesday	10:00 AM – 6:00 PM
Wednesday	10:00 AM – 4:00 PM

Registration Hours

Location: Level 1 Lobby

Saturday	12:00 PM – 5:00 PM
Sunday	7:00 AM – 7:00 PM
Monday	7:00 AM – 7:00 PM
Tuesday	7:00 AM – 6:00 PM
Wednesday	7:00 AM – 1:00 PM

Online Proceedings

To view the proceedings, please visit – https://www.dac.com/proceedings62

Stay Connected

Enjoy complimentary WiFi at DAC:

Wifi Network: DAC2025

Wifi Password: 62DAC2025

First Aid Room

Moscone West First Aid Office is located on the 1st Floor, near the Howard Street entrance (behind registration).

Phone: 415.974.4159

REPORT ALL MEDICAL EMERGENCIES IMMEDIATELY

To report a medical emergency, call 511 on a white house phone, or on a call phone dial 415.974.4021.

DAC Mobile App

You can download the official conference mobile app in the following ways:

- Search your device's App Store for "DAC Conferences"
- Go to the following link: https://www.core-apps.com/dl/62dac
- Once the DAC Conferences application has downloaded, choose "62nd DAC"
- Select to download the event app

Once you are in the app don't forget to set up your profile by going to the Publish My Profile icon. If you click the box to publish your profile your name (and picture if you upload one) will show in the Attendee icon. From there you can make "Friendships" with other attendees which will allow you to send messages, and set up private appointments.

For technical assistance please contact support@core-apps.com

DAC DIRECTORY MAP: LEVEL 1

LEVEL 1 EXHIBIT FLOOR

Exhibits: Aisles 1200 - 1700

DAC Grab 'n Go Concession

Exhibitor Forum

2026 Exhibit Sales Office

Community Connection Zone

Career Development Day (Tuesday, June 24)

LEVEL 1 LOBBY

Registration

DAC DIRECTORY MAP: LEVEL 2

ROOMS 2004, 2011, 2024
Exhibitor Meeting Rooms

ROOM 2006
Hands-on Training Sessions

ROOMS 2008 – 2012
Engineering Track Sessions

LEVEL 2 EXHIBIT FLOOR
Exhibits: Aisles 2100 - 2600

DAC Pavilion

EE Times Chiplet Pavilion

Engineering Track Posters

LEVEL 2 LOBBY
Networking Receptions

Work-in-Progress & Late Breaking Results Posters

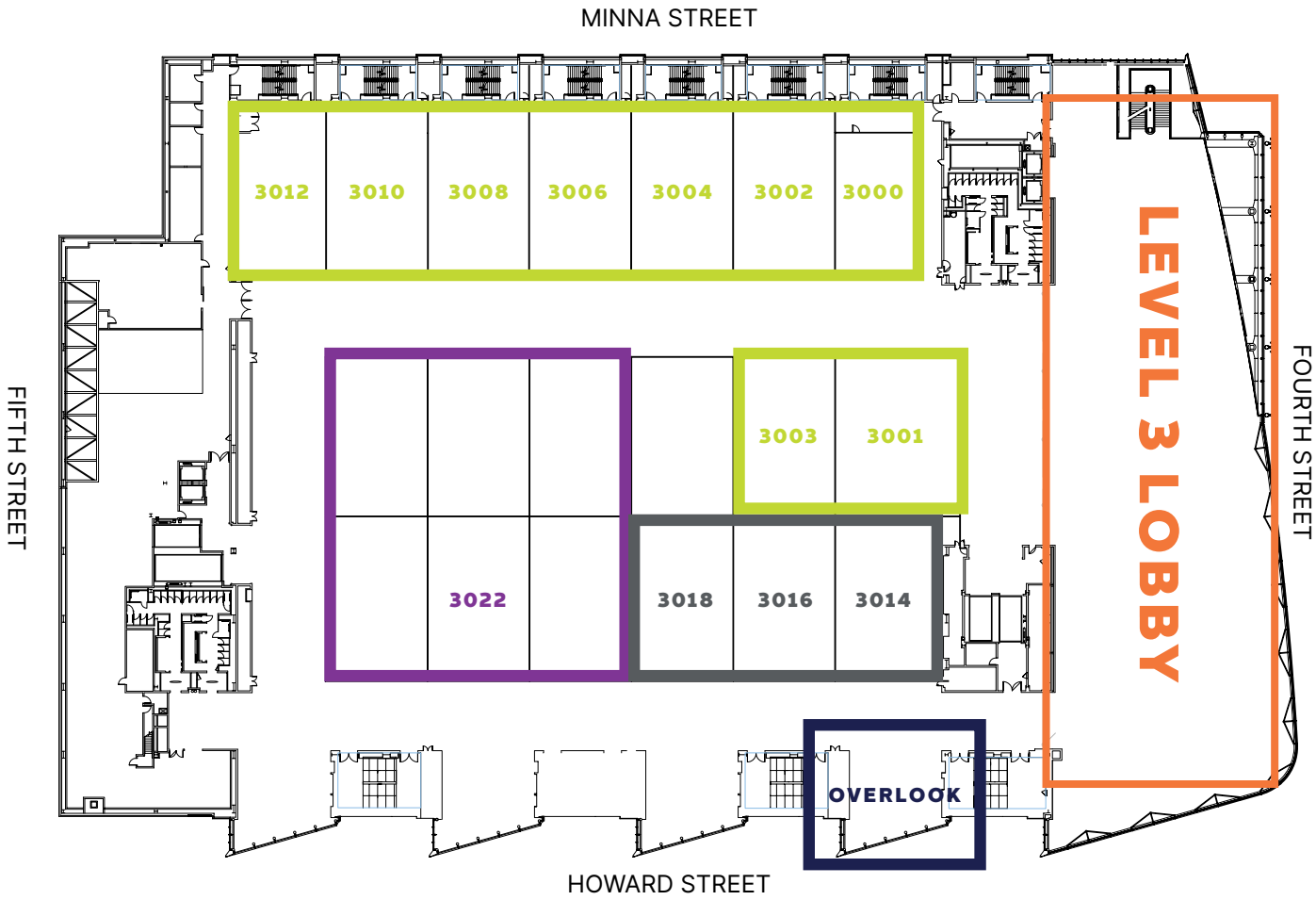
HACK @ DAC

PhD Forum & University Demo

Young Fellows Posters

OVERLOOK
Press Room

DAC DIRECTORY MAP: LEVEL 3



ROOMS 3000-3004, 3006, 3008, 3010, 3012

Research Sessions

Birds of a Feather

Panel Sessions

Special Sessions

Workshops & Tutorials

ROOMS 3014, 3016, 3018

Exhibitor/Sponsor Meeting Rooms

IEEE Council on EDA Distinguished Panel (Tuesday, June 24)

ROOM 3022

Keynote (Monday-Wednesday)

LEVEL 3 LOBBY

Welcome Reception (Sunday, June 22)

Work-in-Progress Posters (Sunday, June 22)

Speaker Breakfast

TPC Reception

OVERLOOK

Speaker Ready Room

IN MEMORIAM

James Boddie, DSP Pioneer (February 1950 – December 2, 2024)

Jim devoted his long career to expanding the world of digital signal processing. His early work in developing signal-processing algorithms on minicomputers with attached array processors led him to cutting-edge signal-processing research at Bell Labs. That work resulted in the development of the DSP1, which AT&T successfully deployed in the 5ESS electronic switch. After the DSP1 project, he held a variety of positions at Bell Labs, AT&T Microelectronics, Lucent Technologies, Agere Systems, and finally StarCore, where he directed the development of increasingly powerful DSP chips.

Robert (Bob) K. Brayton, Professor Emeritus, University of California at Berkeley (October 1933 – January 10, 2025)

Robert K. Brayton, Professor Emeritus of the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley, was a pioneer in logic synthesis and formal verification. With a career spanning over six decades, he made groundbreaking contributions to the field of electronic design automation, authoring over 450 technical papers and 10 books. For the first 26 years of his career, he was a member of the Mathematical Sciences Department at IBM's T.J. Watson Research Center, where he led the Yorktown Silicon Compiler team. His work there helped create one of the most advanced logic synthesis systems of its time. His contributions earned him numerous accolades, including the IEEE CAS Technical Achievement Award and the Phil Kaufman Award. Professor Brayton was known for his inquisitive mind, collaborative spirit, and dedication to mentoring students. His legacy continues to inspire future generations of engineers and researchers. He will be deeply missed by his colleagues, students, and the broader academic community.

Derek Chiou, Professor, University of Texas at Austin (February 1968 – December 26, 2024)

Derek was a frequent contributor / attendee to DAC. He joined the faculty at the University of Texas, Austin (UT), and worked at Microsoft as a Partner Hardware Architect. In 2020, he returned to UT as a full professor and was honored with the Temple Foundation Endowed Teaching Fellowship in Engineering.

Professor Hidetoshi Onodera, Professor Emeritus of Kyoto University, Japan (December 1955 – October 7, 2024)

Hidetoshi Onodera contributed to the EDA field for many years and was an active participant in CEDA. He was Program Chair of ASP-DAC11, General Chair of ASP-DAC12, and SC Chair of ASP-DAC20 through ASP-DAC26.

DAC NETWORKING OPPORTUNITIES

Networking Receptions

Sunday, June 22

Welcome Reception & Work-in-Progress Session

6:00 PM – 7:00 PM | Level 3 Lobby

Monday, June 23

Engineering Track Poster Session

5:00 PM – 6:00 PM | Level 2 Exhibit Hall

Women in Tech Reception, & Work-in-Progress/Late Breaking Results Poster Session

6:00 PM – 7:00 PM | Level 2 Lobby

Tuesday, June 24

Engineering Track Poster Session

5:00 PM – 6:00 PM | Level 2 Exhibit Hall

Networking Reception

6:00 PM – 7:00 PM | Level 2 Lobby

Wednesday, June 25

Engineering Track Poster Session

12:15 PM – 1:15 PM | Level 2 Exhibit Hall

IEEE COUNCIL ON EDA DISTINGUISHED PANEL - 20TH ANNIVERSARY PANEL

AI Hardware & EDA, the next 20 years: Smarter, Taller, Deeper

Date: Tuesday, June 24 | **Time:** 12:00 PM – 1:30 PM | **Location:** 3016/3018, 3rd Floor

Panelist

ALBERTO SANGIOVANNI-VINCENTELLI

EDGAR L. AND HAROLD H. BUTTNER CHAIR OF EECS, UC BERKELEY

Panelist

KUNLE OLUKOTUN

CADENCE DESIGN PROFESSOR OF EE AND CS, STANFORD UNIVERSITY, CO-FOUNDER AND CHIEF TECHNOLOGIST, SAMBANOVA SYSTEMS

Panelist

VAMSI BOPPANA

SENIOR VP AI, AMD

Moderator

SUBHASIS MITRA

WILLIAM E. AYER PROFESSOR OF EE AND CS, STANFORD UNIVERSITY

Moderator

L. MIGUEL SILVEIRA

PRO-RECTOR U LISBOA, PROFESSOR OF ECE, IST TECNICO LISBOA

KEYNOTE PRESENTATIONS

WILLIAM CHAPPELL

VP OF MISSION SYSTEMS, MICROSOFT

The Evolution of Innovation: The Dawn of Reasoning Agents in Chip Design

Monday, June 23 | 8:45 AM - 10:00 AM

The Design Automation Conference (DAC) has long been a beacon for technological foresight and innovation in the semiconductor industry. As we look beyond 2025, the landscape of chip design is poised for another transformative leap with the advent of reasoning agents. This evolution builds upon the foundational milestones set by the Electronics Resurgence Initiative (ERI), which revitalized U.S. semiconductor research, and the integration of cloud computing for silicon. The emergence of Generative AI (GenAI) heralds a new era of creativity and efficiency in design processes across multiple domains.

In this keynote, we will explore how reasoning agents are set to revolutionize the semiconductor industry by offering unprecedented capabilities in problem-solving and decision-making. These agents, drawing inspiration from scientific methodologies in other domains, promise to enhance the precision and speed of design, automate manual tasks, while also fostering a collaborative environment between human designers and AI systems. We will delve into the practical applications of these agents, showcasing their potential to streamline complex design challenges, drive innovation, and increase productivity.

The DAC continues to play a crucial role in this journey, serving as a platform for sharing insights, fostering collaboration, and setting the stage for the next wave of technological advancements. By embracing the synergy between AI and human expertise, we are not only shaping the future of microelectronics but also redefining the boundaries of what is possible in chip design. Join us as we navigate this exciting frontier and explore the opportunities that lie ahead.

ABOUT: Dr. William Chappell is the Vice President and CTO for the Strategic Missions and Technologies Division at Microsoft. As CTO for SMT, he works across the quantum, 5G, mission, space and federal teams to infuse technologies, such as our AI advances, into the product lines, while developing new concepts for the future of the cloud. On the Mission Engineering team in SMT, he developed the Azure Space and Spectrum team, as well as the strategic modeling and simulation team, which includes silicon cloud design.

Prior to Microsoft, he was the director of the Microsystems Technology Office (MTO) for the Defense Advanced Research Projects Agency (DARPA) of the Department of Defense. Serving in this position, he focused the office on three key priorities important to national security. These thrusts included ensuring unfettered use of the electromagnetic spectrum, building an alternative business model for acquiring advanced DoD electronics that feature built-in trust, and developing circuit architectures for next-generation machine learning. MTO creates the MEMS, photonic, and electronic components needed to gracefully bridge the divide between the physical world in which we live and the digital realm where our information resides. Under Dr. Chappell's leadership, MTO developed the basic underpinnings of computation and sensing needed for an effective, information-driven society.

Prior to his work in government, Dr. Chappell was a professor at Purdue University specializing in electromagnetics. Dr. Chappell received his BS, MS, and PhD degrees in Electrical Engineering, all from the University of Michigan.

KEYNOTE PRESENTATIONS continued

MICHAELA BLOTT

SENIOR FELLOW, AMD RESEARCH

Enabling the AI Revolution

Tuesday, June 24 | 8:45 AM - 10:00 AM

The hype surrounding AI has reached unprecedented levels, with governments and industries engaged in an arm's race towards Artificial General Intelligence. As AI permeates every aspect of our lives, from smart sensors and hearing aids to automotive, robotics, and high-energy particle physics, we face a diverse range of challenges that extend far beyond the widely discussed performance scalability and sustainability.

These challenges include demanding requirements such as nanosecond latency, tiny footprints, functional safety, and a high degree of customization.

This talk provides insights into the broad emerging spectrum of AI applications and discusses our latest research demonstrating how these challenges, ranging from bag tagging to 6G, can be addressed through silicon diversity, agile AI stacks and innovative solutions.

ABOUT: Dr. Michaela Blott is a Senior Fellow at AMD Research. She heads a team of international scientists driving groundbreaking research into AI, from robotics to computer architectures, model optimizations and green AI.

Her journey includes a Ph.D. from Trinity College Dublin and a Master's degree from the University of Kaiserslautern, Germany, and brings over 25+ years of experience in leading-edge AI, computer architecture and advanced FPGA design, in research institutions (ETH Zurich and Bell Labs) and development organizations.

She is highly active in the research community as industrial advisor to numerous EU projects and research centres, serves on technical program committees and her contributions to the field were further recognized through multiple Women in Tech Awards.

KEYNOTE PRESENTATIONS continued

JASON CONG

VOLGENAU CHAIR FOR ENGINEERING EXCELLENCE PROFESSOR, UCLA COMPUTER SCIENCE DEPARTMENT

Democratize Chip Design with Deep Learning and Automated Code Transformation

Wednesday, June 25 | 8:45 AM - 10:00 AM

In the past six decades, electronic design automation (EDA) has done a remarkable job to improve the productivity of hardware designers. I would like to argue that the next phase of EDA is to enable many software programmers to design their own chips or accelerators for a wide range of applications for better performance and energy efficiency, which is much needed as we are approaching the end of Moore's Law scaling. In this talk, I shall present our effort towards this goal. Coupled with our multi-decade research high-level synthesis (HLS), we developed and integrated multiple deep learning techniques, such as graph neural networks (GNNs) and large language models (LLMs), cross-modality learning, active learning with cross-entropy minimization, hierarchical mixture of expert modeling, and agent-based design space exploration. For regular structures, such as systolic arrays, stencil computation, or even more general affine programs used almost all deep learning kernel, we can also use mathematical programming to achieve automated code transformation. Combining these techniques, we show very promising results of mapping software code to high-quality silicon implementations.

ABOUT: Jason Cong is the Volgenau Chair for Engineering Excellence Professor at the UCLA Computer Science Department (and a former department chair), with joint appointment from the Electrical and Computer Engineering Department. He is the director of Center for Domain-Specific Computing (CDSC) and the director of VLSI Architecture, Synthesis, and Technology (VAST) Laboratory. Dr. Cong's research interests include novel architectures and compilation for customizable computing, synthesis of VLSI circuits and systems, and quantum computing. He has over 500 publications in these areas, including 19 best paper awards, and 4 papers in the FPGA and Reconfigurable Computing Hall of Fame. He and his former students co-founded AutoESL, which developed the most widely used high-level synthesis tool for FPGAs (renamed to Vivado HLS and Vitis HLS after Xilinx's acquisition). He is member of the National Academy of Engineering, the American Academy of Arts and Sciences, and a Fellow of ACM, IEEE, and the National Academy of Inventors. He is recipient of the SIA University Research Award, the EDAA Achievement Award, the IEEE Robert N. Noyce Medal for "fundamental contributions to electronic design automation and FPGA design methods", and the Phil Kaufman Award for "sustained fundamental contributions FPGA design automation technology, from circuit to system levels, with widespread industrial impact.

SKYTALK PRESENTATIONS

MOHAMED AWAD

SENIOR VICE PRESIDENT AND GENERAL MANAGER, INFRASTRUCTURE LINE OF BUSINESS, ARM

The AI Imperative: What Will We Make of This Moment?

Sunday, June 22 | 5:00 PM - 6:00 PM

ABOUT: Mohamed Awad leads the infrastructure line of business at Arm where he is responsible for leveraging Neoverse's class-leading performance per watt to accelerate Arm's growth across Cloud, HPC, 5G, and the Edge. Previously, Mohamed led Arm's IoT line of business.

Prior to joining Arm, Mohamed spent 10 years in various leadership roles at Broadcom, including establishing the Mixed Signal Asic Products division and building its security and mobile payments business. Before Broadcom, Mohamed served in various leadership roles at Ember Corporation, Lucent Technologies, Nortel Networks, and Avici Systems.

Mohamed has been named inventor or co-inventor on multiple patents throughout his career and holds a BS in Computer Science, from the University of Massachusetts.

JEFF WITTICH

CHIEF PRODUCT OFFICER, AMPERE

AI's Growing Demands: How Artificial Intelligence is Redefining Semiconductor Innovation

Monday, June 23 | 1:00 PM - 1:45 PM | DAC Pavilion, Level 2 Exhibit Hall

The rapid evolution of artificial intelligence is fundamentally reshaping the semiconductor industry. AI workloads demand unprecedented computational power. At the same time, the explosive growth of AI inference is driving energy demands to new heights, forcing the industry to rethink power efficiency at every level – from silicon design to data-center scale optimization. This talk will explore how the demands of AI are reshaping semiconductor innovation, the balance between performance and efficiency, and the advancements that are needed in silicon engineering to power this new era of computing.

ABOUT: Jeff Wittich is the Chief Product Officer at Ampere. Jeff has extensive leadership experience in the semiconductor industry in roles ranging from product and process development to business strategy to marketing. Prior to joining Ampere, he worked at Intel for 15 years in a variety of positions throughout the company. Most recently, he was responsible for the Cloud Service Provider Platform business, driving global market reach, product customization, and ultimately defining the products and platforms being used across the cloud worldwide. While at Intel, Jeff also led a product development team responsible for 5 generations of Xeon processors. He received an Intel Achievement Award for his work in developing the Custom CPU program.

Jeff has an MS in Electrical and Computer Engineering from the University of California, Santa Barbara, and a BS in Electrical Engineering from the University of Notre Dame.

DR. MARK TEHRANIPOOR

CHAIR, ECE DEPARTMENT, UNIVERSITY OF FLORIDA, AND CO-FOUNDER, CASPIA TECHNOLOGIES

New Innovation Frontier with Large Language Models for SoC Security

Tuesday, June 24 | 1:00 PM - 1:45 PM | DAC Pavilion, Level 2 Exhibit Hall

As complex SoCs become prevalent in virtually all systems, these devices also present a primary attack surface. The risks of cyberattacks are real, and AI is making them more sophisticated. As we also deploy AI into the SoC design process, it is imperative that secure design practices are incorporated as well.

Existing security solutions are inadequate to provide effective verification of complex SoC designs due to their limitations in scalability, comprehensiveness, and adaptability. Large Language Models (LLMs) are celebrated for their remarkable success in natural language understanding, advanced reasoning, and program synthesis tasks.

Recognizing this opportunity, we propose leveraging the emergent capabilities of Generative Pre-trained Transformers (GPTs) to address the existing gaps in SoC security, aiming for a more efficient, scalable, and adaptable methodology. In this presentation we offer an in-depth analysis of existing work, showcasing achievements, prospects, and challenges of employing LLMs in SoC security design and verification tasks.

ABOUT: Mark M. Tehranipoor is the Intel Charles E. Young Preeminence Endowed Professor in Cybersecurity at the Department of Electrical and Computer Engineering at the University of Florida. His current research projects include hardware security and trust, electronics supply chain security, IoT security, counterfeit IC detection and prevention, and reliable systems design. He has three patents and has published eight books, 11 book chapters and 350 papers. His projects are sponsored by both the industry (Texas Instruments, Freescale, Comcast, Honeywell, LSI, Mentor Graphics, Juniper, R3Logic, Cisco, Qualcomm, MediaTeck) and the government (NSF, ARO, MDA, DOD, AFOSR, DOE). He is a golden core member of IEEE.

SERGE NICOLEAU

GROUP VICE-PRESIDENT OF TECHNOLOGY, STMICROELECTRONICS

AI Booster for R&D, Edge Computing, Chiplets, and Sustainability

Wednesday, June 25 | 1:00 PM - 1:45 PM | DAC Pavilion, Level 2 Exhibit Hall

Artificial Intelligence (AI) is transforming Research and Development (R&D) by accelerating discovery, optimizing resources, and enhancing decision-making. Edge AI, which processes data closer to its source, reduces latency and energy consumption, promoting sustainability. Chiplet technology, involving smaller integrated circuits combined into larger systems, offers improved performance, scalability, and cost-efficiency. STMicroelectronics is exploring chiplets to advance semiconductor solutions. Amidst climate change, STMicroelectronics is committed to sustainable technologies and responsible products that support decarbonization and digitalization. Integrating AI into R&D, deploying Edge AI, and utilizing chiplets, while addressing sustainability, forms a comprehensive strategy for future advancements, ensuring technological progress and environmental responsibility.

ABOUT: Since 2024, Serge Nicoleau has served as Group Vice-President of Technology at STMicroelectronics, where he is responsible for defining, implementing, and driving the R&D governance of Digital and BCD technologies.

He began his career at STMicroelectronics in 1998, focusing on manufacturing management at the 200mm Crolles fab near Grenoble. Over the years, Serge has held various positions in manufacturing, process engineering, and equipment engineering. In 2004, he joined the Crolles 300mm fab as part of the Crolles2 Alliance between STMicroelectronics, Motorola/Freescale, and Philips/NXP. By 2007, he was promoted to Director of Industrial Technologies, and in 2012, he expanded his responsibilities as Deputy Director of Operations for both the Crolles 200mm and 300mm fabs.

In this role, he tackled the industrial challenges of Automotive and IoT products, working with technologies ranging from 0.5µm to 28nm critical dimensions, including their various variants and options. In 2018, Serge was involved in the new STMicroelectronics 300mm fab program in Agrate, Italy, supporting Smart Power, Analog Mixed Signal, and eNVM products.

In 2020, he assumed the role of General Manager of the Technology & Design Platforms organization, overseeing digital technologies, fast analog technologies, embedded memories, and optical sensors. This organization includes teams in France and India, focusing on the digital products of STMicroelectronics.

Serge Nicoleau holds an Engineering Degree from the Ecole Polytechnique (Paris), a master's degree in Theoretical Physics from the Ecole Normale Supérieure (Lyon), and a PhD in Particle Physics.

TECHTALK PRESENTATIONS

AMIT GUPTA

VICE PRESIDENT & GM, CUSTOM IC & SIEMENS EDA AI

DR. JOHN LINFORD

HEAD OF PRODUCT, CAE/EDA, NVIDIA

Unlocking the Power of AI in EDA

Monday, June 23 | 11:15 AM - 12:00 PM | DAC Pavilion, Level 2 Exhibit Hall

The semiconductor industry is experiencing unprecedented growth, and this growth comes with significant challenges—more design starts, rising design complexities, shorter time-to-market, and a shrinking talent pool. To address these challenges, semiconductor companies are turning to AI-powered EDA solutions. While mainstream AI & GenAI technologies have seen rapid consumer adoption, adapting these AI technologies for EDA use cases is not straightforward due to stringent quality requirements for semiconductor design.

Ideally, EDA AI solutions that provide productivity boosts to chip designers and engineers should (a) seamlessly analyze design and verification data, (b) optimize complex processes, and (c) generate better designs. Across these functional areas, we will discuss illustrative ML, GenAI, and Agentic approaches. Additionally, we will also discuss the challenges associated with AI adoption, including data availability, model interpretability, and computational demands.

Further, we will discuss the grand vision of having a purpose-built centralized EDA AI platform. Such a platform framework can be very powerful by combining sophisticated foundational models or even IC domain-specific foundational models with a multimodal data lake to bring GenAI capabilities to push the boundaries of semiconductor innovation, paving the way for more efficient, scalable, and intelligent design processes.

Join us to explore the capabilities of EDA AI and see what the future holds!

ABOUT: Amit Gupta is a technology executive and serial entrepreneur with over two decades of leadership in semiconductor design automation and AI innovation.

At Siemens EDA, Amit leads the Custom IC division and spearheads AI initiatives across the organization. Under his direction, the team develops cutting-edge AI technologies for the Siemens EDA portfolio, and solutions for variation-aware custom IC design, library characterization, IP validation, simulation, schematic capture, and layout—products that power the chips found in today's most advanced electronic devices.

A proven entrepreneur, Amit founded Solido Design Automation in 2005, and as President & CEO built it into the market leader for AI-based semiconductor design tools before its successful acquisition by Siemens in 2017. Previously, he founded and became President & CEO of Analog Design Automation (1999), which pioneered breakthroughs in circuit design automation and was acquired by Synopsys in 2004.

Amit holds dual degrees in Electrical Engineering and Computer Science with Great Distinction from the University of Saskatchewan.

ABOUT: Dr. John Linford leads NVIDIA's CAE/EDA product team. John's experience spans high-performance physical simulation,

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extreme-scale software optimization, software performance analysis and projection, and pre-silicon simulation and design. Before NVIDIA, John worked at Arm Ltd. where he helped develop the Arm software ecosystem for cloud and HPC. John is based in Austin, TX.

WILLIAM WANG
FOUNDER AND CEO, CHIPAGENTS

Beyond Automation: How Agentic AI is Reinventing Chip Design and Verification

Wednesday, June 25 | 11:15 AM - 12:00 PM | DAC Pavilion, Level 2 Exhibit Hall

Semiconductor innovation is at a critical juncture, demanding next-generational methods to overcome rising complexities, shorter design cycles, and intense competitive pressures. Traditional EDA tools are constrained by manual processes and limited intelligence, but what if we could transcend these limitations?

Enter AI Agents—the AI solution leveraging large language models and advanced algorithms to continue to improve themselves. In this talk, Prof. William Wang, Founder & CEO of ChipAgents, will introduce how AI agents go beyond traditional EDA automation, embedding agentic intelligence capable of independently handling hardware modeling, constraint-solving, automated debugging, testbench generation, and even proactive design optimization. Highlights include Use Cases, Scalability & Reliability: Case studies illustrating substantial productivity improvements, enhanced design quality, and accelerated time-to-market achieved by leading semiconductor enterprises deploying AI Agents. AI Agents in Action: Real-world scenarios demonstrating how AI agents autonomously identify critical bugs, optimize RTL designs, and significantly shorten verification cycles.

ABOUT: William Wang is an internationally recognized pioneer in artificial intelligence and the visionary Founder and CEO behind ChipAgents. He's also Duncan and Suzanne Mellichamp Endowed Chair Professor in AI and Design at UC Santa Barbara. His pioneering research has earned numerous prestigious accolades, including the IEEE Laplace Award, NSF CAREER Award, DARPA Young Faculty Award, the Karen Sparck Jones Award, and IEEE AI's 10 to Watch. William's vision drives ChipAgents' mission to transform semiconductor design through intelligent, agentic AI systems.

ANALYST PRESENTATIONS

DYLAN PATEL

CHIEF ANALYST, SEMIANALYSIS

Accelerator Package and System Design For The AI Era

Monday, June 23 | 10:15 AM - 11:00 AM | DAC Pavilion, Level 2 Exhibit Hall

This session will discuss the design of accelerator packages and systems tailored for the AI era, addressing the need for improved performance, scalability, and energy efficiency to support complex AI workloads.

ABOUT: Through Dylan's dedication and vision, he has grown SemiAnalysis from a solo venture into a highly respected semiconductor market research firm. Since 2020, Dylan has expanded the business into a cohesive, specialized team, with competitive analysis at its core. The company's success has laid the foundation for fully realizing this vision within its new business unit.

JAY VLEESCHHOUWER

SENIOR INDUSTRY ANALYST COVERING ENGINEERING AND ENTERPRISE SOFTWARE, GRIFFIN SECURITIES

A View from Wall Street

Tuesday, June 24 | 10:15 AM - 11:00 AM | DAC Pavilion, Level 2 Exhibit Hall

We will examine the financial performance and key business metrics of the EDA industry through 2024, the further consolidation of EDA (the combination of Synopsys-Ansys), as well as the material technical and market trends and requirements that have influenced EDA business performance and strategies. Among the trends, we will again examine the progression of semiconductor R&D spending and how the market values of the publicly-held EDA companies have evolved. Lastly, we will provide our updated financial projections for the EDA industry for 2025 and 2026.

ABOUT: Mr. Vleeschhouwer has over four decades of research experience. He is a senior industry analyst covering Engineering and Enterprise Software, responsible for fundamental research of companies under coverage, including the regular publication of proprietary company and industry reports and detailed company and industry financial modeling. Principal industry reports include The Software Standard (software industry commentary, news, data, and analysis) and The State of EDA (quarterly in-depth review of Electronic Design Automation). He has appeared multiple times in the Institutional Investor "All-America Research Team" rankings and was ranked by Refinitiv Starmine Analyst Awards (U.S.) #1 in "top stock pickers" for software (2020). He has been regularly invited to present at software and other industry conferences, in addition to broadcast, print and online media appearances.

STEVE GREENFIELD

GENERAL PARTNER, AUTOMOTIVE VENTURES

The Future of Mobility

Wednesday, June 25 | 10:15 AM - 11:00 AM | DAC Pavilion, Level 2 Exhibit Hall

The way we transport humans and cargo is evolving at a pace not experienced since the beginning of the industrial revolution

This session will provide a glimpse into the future of mobility, including grand transportation, marine, aviation and space.

We'll not only discuss vehicle autonomy, electrification and connectivity, but explore how new technologies are impacting other modes of transportation.

ABOUT: Steve has more than 25 years of experience in the automotive technology space. He started his career in 1999 selling software to car dealers and has overseen more than $1 billion in automotive technology acquisitions.

Steve served as TrueCar's Senior Vice President of Strategy and Business Development, and AutoTrader.com's Vice President of Product Management and Business Development, overseeing the acquisitions of vAuto, Kelley Blue Book, HomeNet Automotive, VinSolutions, and DealerScience.

Earlier in his career, Steve served as Manheim's Director of International Development, spearheading Manheim's overseas investments, including establishing new joint ventures in Dubai, Istanbul and Beijing.

He is the author of two books: "The Future of Automotive Retail," and "The Future of Mobility." He is also the author of the Weekly "Intel Report."

For fun, he likes to ride his three motorcycles on the racetrack and hang out with his twelve rescue cats.

DAC AWARDS AND SCHOLARSHIPS

DAC

2025 DAC UNDER-40 INNOVATORS AWARD

In recognition for technical contributions of notable impact in the field of design and automation of electronic circuits and systems

Tsung-Wei Huang, University of Wisconsin, Madison

Tushar Krishna, Georgia Institute of Technology

Xiaolin Xu, Norheastern University

Hajar Falahati, Barcelona Supercomputing Center

Souvik Kundu, Intel Corporation

2025 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

For displaying equality, diversity, and acceptance while visibly helping to advance women in electronic design

Marilyn Wolf, Elmer E. Koch Professor of Engineering at the University of Nebraska, Lincoln

2025 MOST INFLUENTIAL PAPER AWARD

Chisel: constructing hardware in a Scala embedded language, DAC'12

Jonathan Bachrach, UC Berkeley

Huy Vo, UC Berkeley

Brian Richards, UC Berkeley

Yunsup Lee, UC Berkeley

Andrew Waterman, UC Berkeley

Rimas Avižienis, UC Berkeley

John Wawrzynek, UC Berkeley

Krste Asanovic, UC Berkeley

2025 BEST PAPER NOMINEES

INSTA: An Ultra-Fast, Differentiable, Statistical Static Timing Analysis Engine for Industrial Physical Design Applications

LVM-MO: A Large Vision Model Pioneer for Full-Chip Mask Optimization

GEM: GPU-Accelerated Emulator-Inspired RTL Simulation

CirSTAG: Circuit Stability Analysis on Graph-based Manifolds

PICK: An SRAM-based Processing-in-Memory Accelerator for K-Nearest-Neighbor Search in Point Clouds

ZenLeak: Practical Last-Level Cache Side-Channel Attacks on AMD Zen Processors

BoolE: Exact Symbolic Reasoning via Boolean Equality Saturation

ACM/SIGDA

ACM TODAES ROOKIE AUTHOR OF THE YEAR (RAY) AWARD

Enhanced Compiler Technology for Software-based Hardware Fault Detection

Davide Baroffio, Politecnico di Milano, Italy

2025 ACM TODAES BEST PAPER AWARD

VeriGen: A Large Language Model for Verilog Code Generation

Shailja Thakur, New York University, USA

Baleegh Ahmad, New York University, USA

Hammond Pearce, University of New South Wales, Australia

Benjamin Tan, University of Calgary, CA

Brendan Dolan-Gavitt, New York University, USA

Ramesh Karri, New York University, USA

Siddharth Garg, New York University, USA

ACM SIGDA DISTINGUISHED SERVICE AWARD

Sharon Hu, University of Notre Dame

Ulf Schlichtmann, Technical University of Munich

SIGDA SERVICE AWARD

Yuan-Hao Chang, Academia Sinica

Preeti Ranjan Panda, Indian Institute of Technology Delhi

Frank Schirrmeister, Synopsys

Ziegenbein Dirk, Robert Bosch

DAC AWARDS AND SCHOLARSHIPS continued

IEEE/CEDA

2024 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA

For sustained fundamental contributions to Field-Programmable Gate Array (FPGA) design automation technology, from circuit to system levels, with widespread industrial impact.

Prof. Jason Cong, UCLA

IEEE FELLOWS

Umit Ogras, Univerisity of Wisconsin, Madison

Patrick Schaumont, Worcester Polytechnic Institute

Peilin Song, IBM Thomas J. Watson Research Center

Sheldon Tan, University of California, Riverside

IEEE/ACM A RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Luca Carloni, Columbia University

Kenneth L. McMillan, UT Austin

Alberto Sangiovanni-Vincentelli, UC Berkeley

IEEE CEDA OUTSTANDING SERVICE AWARD

For outstanding service to the EDA community as DAC General Chair in 2024

Vivek De, Intel

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

SpikeSim: An End-to-End Compute-in-Memory Hardware Evaluation Tool for Benchmarking Spiking Neural Networks

Abhishek Moitra, Yale University

Abhiroop Bhattacharjee, Yale University

Runcong Kuang, Arizona State University

Gokul Krishnan, Meta Reality Labs

Yu Cao, Arizona State University

Priyadarshini Panda, Yale University

IEEE/CEDA also acknowledges the following awards presented to members of our community

IEEE GUSTAV ROBERT KIRCHOFF AWARD

Prof. Giovanni di Micheli, EPFL

IEEE JUN-ICHI NISHIZAWA MEDAL

Prof. Robert W. Dutton, Stanford University

IEEE JAMES H. MULLIGAN, JR. EDUCATION MEDAL

Prof. Jan Rabaey, UC Berkeley

IEEE COMPUTER SOCIETY EDWARD J. MCCLUSKEY TECHNICAL ACHIEVEMENT AWARD

Prof. Hai (Helen) Li, Duke University

DAC PAVILION SCHEDULE

The location for all events is:
DAC Pavilion | Level 2 Exhibit Hall - Booth #2237

Monday, June 23

10:15 AM - 11:00 AM
ACCELERATOR PACKAGE AND SYSTEM DESIGN FOR THE AI ERA
Speaker: Dylan Patel, SemiAnalysis

11:15 AM - 12:00 PM
UNLOCKING THE POWER OF AI IN EDA
Speakers: Amit Gupta, Siemens; Dr. John Linford, Nvidia

1:00 PM - 1:45 PM
AI'S GROWING DEMANDS: HOW ARTIFICIAL INTELLIGENCE IS REDEFINING SEMICONDUCTOR INNOVATION
Speaker: Jeff Wittich, Ampere Computing

2:00 PM - 2:45 PM
GENERATIVE AI IN DESIGN & VERIFICATION: ARE WE HALLUCINATING OR INNOVATING?
Organizer: Joe Hupcey, Siemens
Moderator: Brian Bailey, Semiconductor Engineering
Panelists: Alon Shtepel, Micron; Abhi Kolpekwar, Siemens

3:00 PM - 4:00 PM
COOLEY'S DAC TROUBLEMAKER PANEL
Moderator:John Cooley, Deepchip
Panelists: Mike Ellow, Siemens; Ravi Subramanian, Synopsys; Paul Cunningham, Cadence Design Systems, Inc.; Dean Drako, IC Manage; Prakash Narain, Real Intent; Sam Appleton, Ausdia

4:00 PM - 4:45 PM
DESIGN, DEVELOP, DOMINATE: THE CHIPS ACT'S ROLE IN SEMICONDUCTOR INNOVATION
Moderator: Nitin Dahad, EE Times Editor
Panelists: Vivek Prasad, NatCast; Nilesh Kamdar, Keysight Technologies; Saverio Fazzari, Senior Lead Engineer/ Engineering Fellow for Microelectronics

5:00 PM - 6:00 PM
POSTER GLADIATOR BATTLE

Tuesday, June 24

10:15 AM - 11:00 AM
VIEW FROM WALL STREET
Jay Vleeschhouwer, Griffin Securities

11:15 AM - 12:00 PM
EXPANDING THE TALENT POOL FOR IC DESIGN THROUGH EXPERIENTIAL LEARNING
Speaker: LaMar Hill, NY Design

1:00 PM - 1:45 PM
NEW INNOVATION FRONTIER WITH LARGE LANGUAGE MODELS FOR SOC SECURITY
Speaker: Mark Tehranipoor, University of Florida, Caspia Technologies

2:00 PM - 2:45 PM
BREAKING THE DESIGN AUTOMATION MOLD: WILD AND CRAZY IDEAS FOR GLOBAL OPTMIZATION
Organizer: Nagesh Gupta, Ilmda.ai
Moderator: Bernard Murphy, SemiWiki
Panelists: Gopal Iyer, Lattice Semiconductor; Vidya Rajagopalan, Rivian; Rajesh Kashyap, Ericsson; Amit Dhir, PWC

3:00 PM - 3:45 PM
AI AND VLSI: A SYMBIOTIC REVOLUTION ENRICHING OUR LIVES AND SHAPING OUR FUTURE
Organizer: Mondira Pant, IEEE TCVLSI Chair - Intel Corporation; Priya Panda, EEE TCVLSI Co-chair - Yale University
Moderator: Ramune Nagisetty, NatCast
Panelists: Manoj Selva, Intel Corporation; Sidney Tsai, IBM; Arijit RayChowdhury, Georgia Institute of Technology; Vijay Raghunathan, Purdue University; Rob Aitken, U.S. Department of Commerce

4:00 PM - 4:45 PM
BUILDING SECURE CHIPS WITHOUT JEOPARDIZING DESIGN BUDGETS AND SCHEDULES
Organizer: Andreas Kuehlmann, Cycuity
Moderator: Andreas Kuehlmann, Cycuity
Panelists: Rachana Maitra, Marvell; Mark Labbato, Booz Allen Hamilton; Vikram Khosa, ARM; Maurizio Paganini, Meta

5:00 PM - 6:00 PM
POSTER GLADIATOR BATTLE

WEDNESDAY, JUNE 25

10:15 AM - 11:00 AM
THE FUTURE OF MOBILITY
Speaker: Steve Greenfield, Automotive Ventures

11:15 AM - 12:00 PM
BEYOND AUTOMATION: HOW AGENTIC AI IS REINVENTING CHIP DESIGN AND VERIFICATION
Speakers: William Wang, ChipAgents

1:00 PM - 1:45 PM
AI BOOSTER FOR R&D, EDGE COMPUTING, CHIPLETS, AND SUSTAINABILITY
Speaker: Serge Nicoleau, STMicroelectronics

3:00 PM - 4:00 PM
POSTER GLADIATOR BATTLE & AWARDS

EXHIBITOR FORUM SCHEDULE

The location for all events is:
DAC Exhibitor Forum | Level 1 Exhibit Hall - Booth #1343

Monday, June 23

10:30 AM - 11:00 AM

TAMING THE WAVEFORM TSUNAMI: AGENTIC AI FOR SMARTER DEBUGGING

Speakers: Zackary Glazewski, ChipAgents.ai; William Wang, ChipAgents.ai

11:15 AM - 11:45 AM

THE GENERATIVE AI REVOLUTION IN SEMICONDUCTOR DEVELOPMENT

Speakers: Prashant Varshney, Microsoft; Richard Paw, Microsoft

12:00 PM - 12:35 PM

BEYOND BREAKING THE BOTTLENECK: SMART VERIFICATION FOR MODERN COMPLEXITY

Speakers: Abhi Kolpekwar, Siemens

1:45 PM - 2:15 PM

STATIC SIGN-OFF METHODOLOGIES: LIBERATING FUNCTIONAL VERIFICATION FROM BOOLEAN SHACKLES

Speakers: Prakash Narain, Real Intent; Kanad Chakraborty, Real Intent; Sanjay Thatte, Real Intent; Lisa Piper, Real Intent; Vikas Sachdeva, Real Intent

2:30 PM - 3:00 PM

MASTERING MODERN DATA MANAGEMENT: INSIGHTS AND CASE STUDIES

Speaker: Pedro Pires, Keysight Technologies

3:30 PM - 4:00 PM

BUILDING TRUST IN GENAI FOR SEMICONDUCTOR DESIGN: ADDRESSING DATA PROVENANCE, QUALITY, AND TRACEABILITY CHALLENGES

Speaker: Vishal Moondhra, Perforce Software

5:00 PM - 5:30 PM

POWERING AI INFRASTRUCTURE WITH INNOVATIONS IN RELIABLE IN SYSTEM/ON-DIE MEMORY DESIGN AND CHARACTERIZATION

Speakers: Ehsan Rashid, Infosys; Chetan Kumar, Infosys; Shreekanth Sampigethaya, Infosys; Kamesh Akundi, Infosys

Tuesday, June 24

10:30 AM - 11:00 AM

INTELLIGENT EXTRACTION OF ADVANCED IC PACKAGE

Speakers: Xiaoyan Xiong, Cadence Design Systems, Inc.; Yingxin Sun, Cadence Design Systems, Inc.; Jiyue Zhu, Cadence Design Systems, Inc.; Gang Kang, Cadence Design Systems, Inc.; Jian Liu, Cadence Design Systems, Inc.

11:15 AM - 11:45 AM

EDA IN THE CLOUD: OPTIMIZING CHIP DESIGN WORKFLOWS WITH GOOGLE CLOUD PLATFORM

Speaker: Sathya Narasimhan, Google

12:00 PM - 12:30 PM

LEVERAGING AI TO BOOST PRODUCTIVITY AND QUALITY OF RESULTS IN THE DIGITAL DESIGN CREATION FLOW

Speaker: Ankur Gupta, Siemens

1:45 PM - 2:15 PM

COVERAGENT: HOW AGENTIC AI IS REDEFINING FUNCTIONAL COVERAGE CLOSURE

Speakers: Mehir Arora, ChipAgents.ai; Zackary Glazewski, ChipAgents.ai; William Wang, ChipAgents.ai

2:30 PM - 3:15 PM

THE RENAISSANCE OF EDA STARTUPS

Speakers: Moshe ZalcbergVeriest, Silicon Catalyst; Priyanka Mathikshara, Voltai; Kanu Gulati, Khosla Ventures; Brian Schechter, Primary Venture Partners; Vinod Kariat, Cadence Design Systems, Inc.

3:30 PM - 4:00 PM

ACCELERATING TAPEOUT BY MONTHS WITH COST-EFFECTIVE PER-MINUTE EDA CLOUD LICENSING

Speakers: Vikram Bhatia, Synopsys;

4:15 PM - 4:45 PM

INDUSTRY-LEADING 3D-IC MULTI-DIE SILICON COMPANIES DISCUSS THEIR MULTIPHYSICS CHALLENGES

Speakers: Murat Becer, Ansys; Sonia Leon, Intel Corporation; Prakhar Mathur, Nvidia; Nitin Navale, Advanced Micro Devices (AMD); Llius Paris, TSMC

4:15 PM - 5:15 PM

A CONFIGURABLE ECAD LIBRARY SOLUTION FOR ALL USERS

Speakers: Julie Liu, Palpilot International

EXHIBITOR FORUM SCHEDULE continued

The location for all events is:
DAC Exhibitor Forum | Level 1 Exhibit Hall - Booth #1343

Wednesday, June 25

10:30 AM - 11:00 AM

GENAI-POWERED CYBER-RESILIENT RTL FOR SECURE AND ROBUST SEMICONDUCTOR DEVICES

Speakers: Peter Levin, Amida Technology Solutions

11:15 AM - 11:45 AM

SIEMENS: ENGINEERING THE SEMICONDUCTOR DIGITAL THREAD

Speakers: Vishal Moondhra, Perforce Software; Michael Munsey, Siemens

1:45 PM - 2:15 PM

DEEPPCB: TRANSFORMING PCB PLACE & ROUTE THROUGH REINFORCEMENT LEARNING

Speakers: Alain-Sam Cohen, InstaDeep

Program accurate as of June 17, 2025.
Locations listed for each speaker are representative of where they live, not where their corporate office is located.

FULL PROGRAM

Sunday, June 22, 2025

POWERING THE FUTURE: MASTERING IEEE 2416 SYSTEM LEVEL POWER MODELING STANDARD FOR LOW-POWER AI AND BEYOND

Time: 9:00 AM - 12:30 PM

Session Type: Half-day Tutorial

Topic Area(s): AI

Room: 3006, Level 3

Description: This half-day tutorial will provide attendees with a comprehensive understanding of the IEEE 2416 standard, used for system level power modeling in the design and analysis of integrated circuits and systems. Through a combination of lectures, discussions, and hands-on exercises, participants will gain practical knowledge and skills necessary to implement and utilize the standard effectively. The workshop will highlight the pressing need for low-power design methodologies, particularly in cutting-edge fields like AI, where computational demands are high. By getting a clear understanding of the IEEE 2416 standard, attendees will be equipped to make decisions on how the standard can be incorporated into their design flow to deliver the efficiencies needed to build their cutting-edge low power designs. The presenters, who are experts from different industry segments (EDA, Foundry, SoC and IP) and academia will use the IEEE2416-2025 version of the standard that is being released at DAC 2025 to explain concepts presented in the workshop.

Organizer(s): Nagu Dhanwada, IBM, US; Leigh Anne Clevenger, Si2, Inc., US

Speakers: Daniel Cross, Cadence Design Systems, Inc., US; Rhett Davis, North Carolina State University, US; Eunju Hwang, Samsung, BE; Pritesh Johari, Qualcomm, US; Akil Sutton, IBM, US

QUANTUM COMPUTING DESIGN AUTOMATION

Time: 9:00 AM - 12:30 PM

Session Type: Tutorial

Topic Area(s): Design

Room: 3004, Level 3

Description: This tutorial provides a comprehensive exploration of design automation for quantum computing, structured into three focused sections, each addressing critical challenges and advancements in the field. With quantum computing poised to revolutionize technology, the efficient design and optimization of quantum systems are imperative for scaling, performance enhancement, as well as sustainability.

Organizer(s): Hanrui Wang, University of California, Los Angeles, US; Zhiding Liang, Rensselaer Polytechnic Institute, US

Speakers: Yiran Chen, Duke University; Weiwen Jiang, George Mason University; Siyuan Niu, Lawrence Berkeley National Lab; Daniel Tan, Harvard; Thomas W. Watts, HRL Labs

THE 2ND INTERNATIONAL WORKSHOP ON DEEP LEARNING -- HARDWARE CO-DESIGN FOR GENERATIVE AI ACCELERATION

Time: 9:00 AM - 12:30 PM

Session Type: Workshop

Topic Area(s): AI

Room: 3003, Level 3

Description: In the rapidly evolving domain of computational technologies, the transformative impact of artificial intelligence (AI) continues to shape the future. DCgAA 2025 builds on the success of its inaugural edition by diving deeper into the frontier of deep learning (DL) and hardware co-design, with an amplified focus on real-world deployment challenges and next-generation innovations for generative AI applications. This second iteration emphasizes expanding the scope beyond foundational discussions, addressing emerging paradigms in generative AI, including multimodal fusion, real-time adaptive processing, and decentralized edge applications. Acknowledging the growing role of foundation models, diffusion models, and large-scale generative systems, this workshop prioritizes optimizing these technologies for sustainable scalability—balancing performance, energy efficiency, and accessibility across diverse computing environments such as edge devices, AR/VR platforms, and ubiquitous IoT systems. Through a blended format of keynotes, paper presentations, interactive discussions, and novel program additions, DCgAA 2025 seeks to redefine the boundaries of DL-hardware integration. By engaging thought leaders, researchers, and practitioners across academia and industry, this workshop promises to set new benchmarks for hardware-aware generative AI, driving innovation that is efficient, scalable, and impactful in the real world.

Organizer(s): Dongkuan Xu, North Carolina State University, US; Tinoosh Mohsenin, University of Maryland, Baltimore County, US; Caiwen Ding, University of Minnesota Twin Cities, US; Hua Wei, Arizona State University, US; Ang Li, University of Maryland, US; Peipei Zhou, Brown University, US; Yingyan (Celine) Lin, Georgia Institute of Technology, US; Yanzhi Wang, Northeastern University, US

IN-MEMORY ARCHITECTURES AND COMPUTING APPLICATIONS WORKSHOP (IMACAW) - 4TH EDITION

Time: 9:00 AM - 12:30 PM

Session Type: Workshop

Topic Area(s): Design

Room: 3002, Level 3

Description: Modern computer architectures and the device technologies used to manufacture them are facing significant challenges, limiting their ability to meet the performance demands of complex applications such as Big Data processing and Artificial Intelligence (AI). The In-Memory Architectures and Computing Applications Workshop (iMACAW) workshop seeks to provide a platform for discussing In-Memory Computing (IMC) as an alternative architectural approach and its potential applications. Adopting a cross-layer and cross-technology perspective, the workshop will cover state-of-the-art research utilizing various memory technologies, including SRAM, DRAM, FLASH, RRAM, PCM, MRAM, and FeFET. Additionally, the workshop aims to strengthen the IMC community and offer a comprehensive view of this emerging computing paradigm to design automation professionals. Attendees will have the opportunity to engage with invited speakers, who are pioneers in the field, learn from their expertise, ask questions, and participate in panel discussions.

Organizer(s): Deliang Fan, Arizona State University, US; Nima TaheriNejad, Heidelberg University, DE; Wantong Li, University of California, Riverside

3RD AI/CAD FOR HARDWARE SECURITY WORKSHOP (AICAD4SEC 2025)

Time: 9:00 AM - 5:00 PM

Session Type: Workshop

Topic Area(s): AI, Security

Room: 3001, Level 3

Description: Security vulnerabilities in hardware designs are catastrophic as once fabricated, they are nearly impossible to patch. Modern SoCs (Systems-on-Chip) face threats like side-channel leakage, information leakage, access control violations, and malicious functionality, jeopardizing the foundational integrity of SoCs. These vulnerabilities circumvent software-level defenses, creating urgent challenges for hardware security. Ensuring the security of hardware designs is challenging due to their huge complexity, aggressive time-to-markets, and the variety of attacks against hardware designs. Moreover, it is very costly for a design house to keep many security experts with in-depth design knowledge with diverse security implications. So, the semiconductor industry looks for a set of metrics, reusable security solutions, and automatic computer-aided-design (CAD) tools to aid analysis, identifying, root-causing, and mitigating SoC security problems.

Artificial Intelligence (AI) is revolutionizing the landscape of CAD, providing unprecedented opportunities to tackle these challenges. AI-driven tools have the potential to analyze complex SoC designs at multiple abstraction levels, automatically detect vulnerabilities, and even predict potential attack vectors. By leveraging advanced AI models, including large language models (LLMs) and machine learning algorithms, we can now accelerate the identification of root causes, assess risks, and recommend security countermeasures. The inclusion of AI in CAD/EDA for security addresses these issues in innovative ways, e.g., (1) Enhanced Vulnerability Detection, (2) Contextual Adaptability, and (3) Proactive Security.

Building on the resounding success of the 1st (inauguration) and 2nd CAD4Sec workshops, co-located with the DAC'59 (2022) and DAC'60 (2023), respectively, and drawing ~100 attendees each year, the 3rd iteration aims to embrace the transformative intersection of AI, CAD, and hardware security. Now rebranded as AICAD4Sec, this workshop aims to drive innovation at the nexus of AI-driven solutions and hardware design security. The ultimate vision of AICAD4Sec is to establish a cutting-edge platform that shows advancements and sets the roadmap for secure, AI-enabled hardware design, specifically, (i) Engaging experts from industry leaders like Google, Microsoft, Synopsys, and ARM, alongside academia and government agencies such as DARPA and AFRL; (ii) Showcasing the latest breakthroughs in AI-enhanced CADs for security; (iii) Facilitating practical demonstrations of AI-driven solutions in hardware security by both industries/academia; and (iv) Hosting a dynamic panel discussion on the evolving role of AI, with a particular focus on large language models and their implications for secure SoC design.

Building on the foundation of its predecessors, the 3rd AICAD4Sec workshop will contain several technical talks on the scope of metrics and CAD as the following:

- CAD Tools for Side-Channel Vulnerability Assessment (Power, Timing, and Electromagnetic Leakage)
- Security-Oriented Equivalency Checking and Property Validation
- Fault Injection Analysis and Countermeasure Integration in CAD
- CAD for Secure Packaging and Heterogeneous Integration
- Assessment of Physical Probing and Reverse Engineering Risks
- AI-Powered Tools for Pre-Silicon Vulnerability Mitigation and Countermeasure Suggestions
- Large Language Models for Security-Aware Design Automation
- ML-Enhanced Threat Detection Across Design Abstractions
- AI-Augmented Detection of Malicious Functionality in Hardware Designs
- AI-Enabled Security Verification for Emerging SoC Architectures

Organizer(s): Farimah Farahmandi, University of Florida; Hadi Mardani Kamali, University of Central Florida; Mark Tehranipoor, University of Florida

WORKSHOP ON CHIPLET-BASED HETEROGENEOUS INTEGRATION AND CO-DESIGN (CHICO)

Time: 9:00 AM - 5:00 PM

Topic Area(s): Design

Session Type: Workshop

Room: 3000, Level 3

Description: Contemporary microelectronic design is facing tremendous challenges in memory bandwidth, processing speed and power consumption. Although recent advances in monolithic design (e.g. near-memory and in-memory computing) help relieve some issues, the scaling trend is still lagging behind the ever-increasing demand of AI, HPC and other applications. In this context, technological innovations beyond a monolithic chip, such as 2.5D and 3D packaging at the macro and micro levels, are critical to enabling heterogeneous integration with various types of chiplets and bringing significant performance and cost benefits for future systems. Such a paradigm shift further drives new innovations on chiplet IPs, heterogeneous architectures and system mapping.

This workshop is designed to be a forum that is highly interactive, timely and informative, on the related topics:

- Roadmap and technology perspectives of heterogeneous integration
- IP definition for chiplets
- Signaling interface cross chiplets
- Network topology for data movement
- Design solutions for power delivery
- Thermal management
- Testing in a heterogeneous system
- High-level synthesis for the chiplet system
- Architectural innovations
- Ecosystems of IPs and EDA tools

The format of the workshop will consist of multiple invited presentations from industry, academia, and government funding agencies. We will also organize a panel for discussions. Intended audience includes industry and academic researchers, funding agencies, IP providers, EDA tool vendors, and foundry engineers.

Organizer(s): Yu Cao, University of Minnesota, US; Puneet Gupta, University of California, Los Angeles, US

EVEN HIGHER-LEVEL SYNTHESIS: AN EXPLORATION OF AI HARDWARE ACCELERATORS USING HLS4ML

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Tutorial

Room: 3006, Level 3

Description: With the rise of artificial intelligence, the popularization of deep learning, and a constantly evolving industry, the demand for flexible and efficient tools has never been greater. As algorithms grow more complex, their runtime and energy consumption increase exponentially. Customized hardware accelerators, long used for specific mathematical operations, remain essential for managing modern applications' computational and power demands. Hardware accelerators can speed up complex computations by orders of magnitude, but their manual design and verification processes are often challenging and time-consuming.

High-Level Synthesis (HLS) provides a solution by transforming high-level algorithm descriptions, typically written in C or C++, into synthesizable RTL suitable for hardware implementation. This approach reduces development time for RTL engineers while offering flexibility beyond what traditional handwritten RTL can provide. We extended this capability to the machine learning domain with the open-source framework hls4ml, which allows neural networks trained in Python frameworks like Tensorflow or PyTorch to be synthesized into efficient hardware representations for the traditional FPGA and ASIC flows. This breakthrough addresses the growing need for reduced design turnaround and easy verification of ML hardware accelerators with low latency and power efficiency constraints.

During this tutorial, we will demonstrate how Python complements HLS by simplifying the ML design process, bridging the gap between software and hardware development. Attendees will explore how we translate neural networks modeled in Python into fixed-point C++ models suitable for HLS workflows. We will dive into strategies like Value-Range Analysis and Quantization-Aware Training, which optimize these designs for deployment and evaluate their accuracy, power consumption, and energy efficiency.

Organizer(s): Mathilde Karsenti, Siemens, US

Speakers: Cameron Villone, Siemens EDA, US; Giuseppe Di Guglielmo, Fermilab, US

INTRODUCTION TO FOUNDATION AI MODEL AND ITS EDA APPLICATIONS

Time: 1:30 PM - 5:00 PM

Topic Area(s): AI

Session Type: Tutorial

Room: 3004, Level 3

Description: The objectives of this tutorial are to provide a solid foundation in understanding large language models and their applications, equip participants with the trending AI knowledge to apply self-supervised learning techniques effectively in their own target applications, demonstrate the integration of multimodal data for enhanced AI capabilities, and discuss strategies to improve the efficiency of large-scale models. This tutorial content is designed for researchers, industry practitioners, and students interested in the latest advancements in AI model development and deployment. Our target audience may work in different backgrounds, including but not limited to: EDA researchers or engineers, especially those interested in AI for EDA; computer architecture researchers or engineers, especially those working on AI accelerator design; algorithm researchers or engineers, especially those working on AI algorithms, applications, and products. The tutorial will cover basic large language model (LLM) techniques, including transformer and RAG, self-supervised pretraining techniques, such as contrastive learning, multimodal representation learning, the efficiency of large foundation models, and foundation AI model's applications in EDA

Organizer(s): Xiaoxuan Yang, University of Virginia, US.

Speakers: Zhiyao Xie, Hong Kong University of Science and Technology (HKUST), HK ; Wei Wen, Meta, US; Ang Li, The University of Maryland, College Park, US; Zhiyao Xie, Hong Kong University of Science and Technology (HKUST), CN

FIRST INTERNATIONAL WORKSHOP ON SYNERGIZING AI AND CIRCUIT-SYSTEM SIMULATION

Time: 1:30 PM - 5:00 PM

Topic Area(s): Design

Session Type: Workshop

Room: 3003, Level 3

Description: Hardware tape-outs are prohibitively expensive and time-consuming, making circuit and system (CAS) simulators crucial for verifying designs efficiently and cost-effectively prior to fabrication. An extensive array of simulators exists today, tailored for various CAS applications, such as Verilog simulators for digital integrated circuits (ICs), SPICE-based simulators for analog ICs, Verilog-AMS simulators for mixed-signal systems, and electromagnetic simulators for high-frequency circuits and antennas. Despite decades of development and the high degree of maturity achieved by CAS simulators, the recent surge of artificial intelligence (AI) is rekindling renewed interest from both software and hardware perspectives. On the hardware front, the exceptional parallelism capabilities of GPUs can be harnessed to expedite CAS simulations, such as GPU-accelerated SPICE simulations and logic gate simulation. On the software side, deep learning (DL) algorithms are being seamlessly integrated into CAS simulators serving as surrogate models or providing initial guesses, to reduce computational workloads and improve efficiency. Conversely, the principles of CAS simulation are catalyzing novel AI models. One prominent example is the use of ordinary differential equations (ODEs), which have long been a cornerstone of time-domain analog circuit simulations in SPICE, with the adjoint method used for gradient computations. In the DL community, these techniques have evolved into Neural ODEs, a class of models that parameterize ODE dynamics using neural networks. Neural ODEs have proven especially effective for time-series forecasting and are closely linked to the development of generative diffusion models. Similarly, state-space models (SSMs), once the bedrock of linear time-invariant systems, now underpin architectures such as Mamba, designed for efficient natural language processing. Another notable adaptation of classical circuit principles in modern AI is Kirchhoff's current law (KCL), which has been leveraged to construct analog neural networks, such as memristor crossbar arrays and KirchhoffNet. Furthermore, Fourier transforms, widely used in frequency-domain CAS simulations for signal processing, have been reimagined as neural operators. This adaptation has led to breakthroughs in AI-driven scientific applications, such as weather forecasting.

The similarities between CAS simulation and AI are profound, yet no dedicated platform exists for researchers, engineers, and practitioners to discuss this interdisciplinary topic. Recognizing this critical need, the First International Workshop on Synergizing AI and Circuit-System Simulation aims to bring together experts to explore innovative methodologies that leverage the synergies between these fields. The workshop will provide a platform to discuss recent advancements and foster interdisciplinary collaboration.

Organizer(s): Zhengqi Gao, Massachusetts Institute of Technology, US; Duane Boning, MIT, US; Zhou Jin, Super Scientific Software Laboratory, Dept. of CST, CN University of Petroleum-Beijing, CN; Yanqing Zhang, Nvidia, US; Haoxing Ren, Nvidia Corporation, US; Yiran Chen, Duke University, US; Ron Rohrer, CMU, US

NSF WORKSHOP ON HARDWARE ATTACK ARTIFACTS, ANALYSIS, AND METRICS (WHAAAM)

Time: 1:30 PM - 5:00 PM

Topic Area(s): Security

Session Type: Workshop

Room: 3002, Level 3

Description: The Workshop on Hardware Attack Artifacts, Analysis, and Metrics (WHAAAM) aims to promote open and practical contributions that improve our ability to reason about offensive hardware security. Over the past decade, we've observed the repeated discovery of real-world hardware vulnerabilities. No longer a theoretical exercise, hardware attacks are developed by multinational corporations and nation states with devastating consequences. Responses from both academia, industry, and government agencies has grown as a result. However, we still fall-short in our ability to defend against creative malicious actors. This is in part due to an existing gap between academic threat modelling and PoCs versus end-to-end attacks. WHAAM seeks to bridge this gap in the hardware security research community, by seeking open and artifact-driven submissions that that grows our understanding of practical attacker capabilities, as well as robust responses based on empirical root-cause analysis and quantitative metrics. Importantly, as opposed to competition-based hardware security events (Hack@DAC, IEEE HOST) that have limited focus, WHAAAM encourages a diverse and creative outlet for student researchers to demonstrate a range of cutting-edge work in a hands-on environment.

Organizer(s): Dean Sullivan, University of New Hampshire, US; Vincent Immler, Oregon State University, US

EMERGING TECHNOLOGY APPLICATIONS ON PERSONALIZED EDGE LLMS

Time: 3:30 PM - 5:00 PM

Topic Area(s): AI

Session Type: Tutorial

Room: 3006, Level 3

Description: Edge-based Large Language Models (edge LLMs) can preserve the promising abilities of LLM while ensuring user data privacy. Additionally, edge LLMs can be utilized in various fields without internet connectivity constraints. However, edge LLMs face significant challenges in training, deployment, and inference. Limitations in memory storage, computational power, and data I/O operations can hinder the deployment of advanced LLMs on edge devices. These constraints often result in poor performance in customization, real-time user interaction, and adaptation to novel situations. Traditional acceleration methods, primarily designed for advanced computation platforms, may not be optimal for all types of edge devices. As a complementary solution, Compute-in-Memory (CiM) architectures based on emerging non-volatile memory (NVM) devices offer promising opportunities. These architectures, having demonstrated numerous advantages in traditional neural networks, can help overcome the computational memory bottleneck of edge devices and reduce competition for core computational resources. Through the introduction of software-hardware co-design and co-optimization methods, NVCiM can significantly enhance edge LLM performance in resource-limited environments. Moreover, NVCiM-based edge LLM systems are more cost-effective compared to LLMs running on high-performance computing devices. This makes them suitable for various personalized applications, particularly in healthcare and medical fields.

Organizer(s): Ismail Bustany, AMD, US

Speakers: Yiyu Shi, University of Notre Dame, US; Jinjun Xiong, University at Buffalo, US

SUNDAY WORK-IN-PROGRESS POSTER RECEPTION

Time: 6:00 PM - 7:00 PM

Session Type: Work-in-Progress Poster

Room: Level 3 Lobby

3D-IC STACKING AND FLOORPLAN DESIGN METHODOLOGY THROUGH ML-BASED PRE-TRAINED MODEL AND PRACTICAL MACRO PLACEMENT FRAMEWORK FOR PERFORMANCE AND THERMAL CO-OPTIMIZATION

Yu-Wei Tseng, Po-Hsiang Huang, Wei-Yi Willy Hu, Intel, US

A FAST AND ACCURATE THERMAL SOLVER FOR CHIP THERMAL THROTTLING ANALYSIS

Shinyu Shiau, Sainan Lu, Stimit Shah, Xin Ai, Yun Dai, Cadence Design Systems, Inc., US

A GRAPH-BASED APPROACH FOR OPTIMIZING PIN ACCESS IN NANOSHEET FET STANDARD CELL LIBRARY SYNTHESIS

Meng-Yu Shih, Yih-Lang Li, National Yang Ming Chiao Tung University, TW

A RETINA-INSPIRED PATHWAY TO REAL-TIME MOTION PREDICTION INSIDE IMAGE SENSORS FOR EXTREME-EDGE INTELLIGENCE

Subhradip Chakraborty, Md Kaiser, Akhilesh Jaiswal, University of Wisconsin Madison, US; Shay Snyder, Maryam Parsa, George Mason University, US; Gregory Schwartz, Northwestern University, US

A SCALABLE TWO-STEP APPROACH TO OPTIMIZE DATA AND ENERGY MIGRATIONS IN MINI DATA CENTERS FOR CARBON-NEUTRAL COMPUTING

Kazuki Okazawa, Hiroki Nishikawa, Dafang Zhao, Ittetsu Taniguchi, Takao Onoye, Osaka University, JP; Marcos da Silva, Independent Researcher, FR; Abdoulaye Gamatie, LIRMM, FR

ACCELERATING CLUSTERING ALGORITHMS FOR LARGE-SCALE DATASETS VIA COLLABORATIVE GPU AND CXL-MEMORY ARCHITECTURE

Taehyung Park, Hyuk-Jae Lee, Seoul National University, KR; Chae Eun Rhee, Hanyang University, KR

ACCELERATING DEVICE LEVEL SYNTHESIS OF BINARIZED CONVOLUTIONAL NEURAL NETWORKS

Francisco Andreo-Oliver, Gines Domenech-Asensi, Ramon Ruiz-Merino, Universidad Politecnica de Cartagena, ES; Jose Diaz-Madrid, Centro Universitario de la Defensa - UPCT, ES

ADAMAP: ADAPTIVE HARDWARE MAPPING FOR MODEL COMPRESSION USING LOW-RANK DECOMPOSITION

Priyansh Bhatnagar, Rishabh Kumar, Pranav Raj, Mingu Kang, University of California, San Diego, US

ADORA: AN ARITHMETIC AND DYNAMIC OPERATION RECONFIGURABLE ACCELERATOR USING IN-MEMORY LOOK-UP TABLES

Stefan Maczynski, Mark Indovina, Sathwika Bavikadi, Amlan Ganguly, Rochester Institute of Technology, US; Purab Sutradhar, Boise State University, US; Sai Manoj Pudukotai Dinakarrao, George Mason University, US

AI-ENABLED EFFICIENT EXTRACTION OF ENTIRE ADVANCED IC PACKAGE

Xiaoyan Xiong, Yingxin Sun, Jiyue Zhu, Gang Kang, Jian Liu, Cadence Design Systems, Inc., US

ALPHASPARSETENSOR: DISCOVERING FASTER SPARSE MATRIX MULTIPLICATION ALGORITHMS ON GPU FOR LLM INFERENCE

Xuanzheng Wang, Shuo Miao, Zihan Zhu, Peng Qu, Youhui Zhang, Tsinghua Univ., CN

AN ADVANCED WAIT-FREE PROTOCOL FOR DATA COMMUNICATION AND CONSISTENCY IN MULTI-CORE REAL-TIME EMBEDDED SYSTEMS

Dong Li, Sen Wang, Adhip Shukla, Haibo Zeng, Virginia Tech, US; Yuchen Zhou, Khaja Shazzad, General Motors, US

APPROXIMATION-BASED INTER-PE COMMUNICATION-FREE IMAGE FILTERING FOR COMMODITY PIM

Chan Lee, Shinnung Jeong, Heelim Choi, Jaeho Lee, Haeeun Jeong, Hoyun Youm, Ju Min Lee, Hanjun Kim, Yonsei University, KR

AUTOMATED HARDWARE-MAPPING CO-DESIGN FOR NEURAL NETWORK ACCELERATION WITH SINGLE-STEP REINFORCEMENT LEARNING

Yifeng Xiao, University of Southern California, US; Yurong Xu, Ning Yan, Masood Mortazavi, Futurewei, US; Pierluigi Nuzzo, University of California, Berkeley, US

AUTOMATING RTL GENERATION USING AGENTIC LLMS

Athmanarayanan Lakshmi Narayanan, Mahesh Subedar, Omesh Tickoo, Intel, US

AUTOMOTIVE REMOTE DIRECT MEMORY ACCESS (ARDMA) FOR SOFTWARE DEFINED VEHICLE (SDV)

Nithya Somanath, Bhagyashri Katti, Zachary Steigerwald, Khaja Shazzad, Markus Jochim, Yuchen Zhou, Steve DiBella, General Motors, US

BANK-SPLIT PIM: ENABLING CONCURRENT PIM AND MEMORY OPERATIONS FOR LLM INFERENCE IN HETEROGENEOUS SYSTEMS

Hyeongjun Cho, Yoonho Jang, Seokin Hong, Sungkyunkwan University, KR

BEYOND VERILOG: AGENTS FOR EMERGING HDLS

Farzaneh Rabiei Kashanaki, Mark Zakharov, Jose Renau, University of California, Santa Cruz, US

BLAQSMITH: RESOLVING TWO-QUBIT GATE COUNT EXPLOSION IN T-COUNT-OPTIMIZED QUANTUM CIRCUITS

Mu-Te Lau, Hsiang-Chun Yang, Hsin-Yu Chen, Chung-Yang (Ric) Huang, National Taiwan University, TW

SUNDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

CARBONSET: A DATASET TO ANALYZE TRENDS AND BENCHMARK THE SUSTAINABILITY OF CPUS AND GPUS

Jiajun HU, Chetan Choppali Sudarshan, Maxwell Clifford, Vidya A. Chhabria, Aman Arora, Arizona State University, US

CIS: IN-STORAGE COMPRESSION FOR IMPROVING READ PERFORMANCE OF NAND FLASH-BASED SSDS

Minjin Park, Minkyu Choi, Seongwook Kim, Junbum Park, Joonseong Hwang, Seokin Hong, Sungkyunkwan University, KR

COMBINING PHYSICS-INFORMED AND DATA-DRIVEN LEARNING FOR EFFICIENT MODELING OF MEMRISTIVE DEVICES

Zihan Zhang, Marco Donato, Tufts University, US

DAEDALUS: A FLOORPLANNING STRATEGY FOR NEXT-GENERATION 3D CHIPLET INTEGRATION

Sebastiano Gaiardelli, Michele Lora, Franco Fummi, University of Verona, IT; Marco Cignarella, Anna Fontanelli, Francesco Rossi, Michele Taliercio, Monozukuri S.p.A, IT

DEEP CO-DESIGN OF A 7.461 TOPS/W/MM^(2) CGRA FOR EDGE-BASED PERCEPTION APPLICATIONS

Rohit Prasad, Pascal Aubry, Tiana Rakotovao, Kods Trabelsi, CEA, FR

DESIGN GUIDELINES OF SUCCINCT PULSE GENERATORS FOR SCALABLE SUPERCONDUCTING QUBIT CONTROLLERS

Ryosuke Matsuo, Kazuhisa Ogawa, Hidehisa Shiomi, Makoto Negoro, Takefumi Miyoshi, Jun Shiomi, The University of Osaka, JP;Ryutaro Ohira, QuEL, Inc., JP; Michihiro Shintani, Kyoto Institute of Technology, JP; Hiromitsu Awano, Takashi Sato, Kyoto University, JP

DESIGN-AWARE MULTI-ARMED BANDIT APPROACH FOR AUTOMATED DESIGN VERIFICATION

Lorenzo Ferretti, Surya Bandlamudi, Nihar Athreyas, Vikram Narayan, Samir Mittal, Micron Technology, US

DESIGNING AND EVALUATING HBM-AWARE NTT ACCELERATOR

Sangwon Shin, Son Pham, Taeweon Suh, Korea University, KR; Lei Xu, Kent State University, US; Weidong Shi, University of Houston, US

DUALMAP: ENHANCING EFFICIENCY FOR IN MEMORY COMPUTING WITH DUAL STRATEGIES OF KERNEL DUPLICATION AND COMPACTION

Wenxin Wang, Meng Pang, Peng Qu, Youhui Zhang, Tsinghua University, CN

DYNAMIC FPGA ACCELERATION FOR CLOUD WORKLOADS: A HLS-BASED JIT COMPILATION APPROACH

Rui Li, Shuang Cao, Dawn Computing, US

EARLY MISMATCH DETECTION IN ANALOG LAYOUT USING PLS NETLIST

Abhishek Jain, Ashutosh Singh, Anil Kumar, Krish Singh, STMicroelectronics, IN

EFFICIENTLY EXPLOITING INFERENCE PARALLELISM IN TWO-SIDED SPARSE CNNS FOR A HIGH-SPEED, LOW-COST ACCELERATOR

Son Pham, Sangwon Shin, Taeweon Suh, Korea University, KR; Lei Xu, Kent State University, US; Weidong Shi, University of Houston, US

EHPC: EFFICIENT HETEROGENEOUS PROBABILISTIC COMPUTING ARCHITECTURE FOR FLOORPLANNING ACCELERATION

Weican Chen, Chenhao Xia, Guanwen Yao, Haoxuan Wang, Fei Liu, Peking University, CN

EMSTRANS: AN EFFICIENT HARDWARE ACCELERATOR FOR TRANSFORMER WITH MULTI-LEVEL SPARSITY AWARENESS

Dingyang Zou, Qiye Ding, Zhongfeng Wang, Nanjing University, CN; Baichen Chen, Liang Xu, Meiqi Wang, Sun Yat-Sen University, CN

ENABLING SYSTOLIC COMPUTING ON ELASTIC COARSE-GRAINED RECONFIGURABLE ARRAY FOR HPC AND AI

Chenlin Shi, Teng, Shinobu Miwa, The University of Electro-Communications, JP; Boma Adhi, Kentaro Sano, RIKEN Center for Computational Science, JP

EQBAB: EFFICIENT EQUIVALENCE VERIFICATION FOR COMPRESSED DNNS WITH BOUND PROPAGATION

Zihao Mo, Weiming Xiang, Augusta University, US; Yejiang Yang, Southwest Jiao Tong University, CN

EXTENDING RISC-V BASED GPGPU FOR FAST EXECUTION OF REGULAR DATA-INTENSIVE KERNELS

Giuseppe Sarda, Nimish Shah, Marian Verhelst, KU Leuven, BE; Abubakr Nada, Debjyoti Bhattacharjee, imec, BE

FAST SIMULATION ALGORITHM FOR NEGATIVE-CAPACITANCE FINFET BASED ON LATENCY INSERTION METHOD

Yi Zhou, José Schutt-Ainé, University of Illinois at Urbana-Champaign, US

FLOWGUARD: TOWARDS RELIABLE DNN ACCELERATORS VIA FINE-GRAINED FAULT TOLERANCE IN SYSTOLIC ARRAY

Sihyung Kim, Gwangeun Byeon, Seongwook Kim, Junbum Park, Seokin Hong, Sungkyunkwan University, KR

GAIA: A GENERATIVE AI APPROACH FOR ENABLING AIRCRAFT DIGITAL TWIN CREATION

Francesco Biondani, Luigi Capogrosso, Nicola Dall'Ora, Marco Cristani, Franco Fummi, University of Verona, IT; Enrico Fraccaroli, University of North Carolina at Chapel Hill, IT; Domenico Migliore, Francesco Acerra, Leonardo S.p.A., IT

SUNDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

GENERATOR OF CONSTRAINED TEST PATTERN BASED ON MULTI-SCALE GRADIENT GENERATIVE ADVERSARIAL NETWORKS

Yajuan Su, Tianyang Gai, CN; Xiaojing Su, Xin Hong, Pengyu Ren, Yujie Jiang, Yayi Wei, Institute of Microelectronics of Chinese Academy of Sciences, CN

GRACO - A GRAPH COMPOSER FOR INTEGRATED CIRCUITS

Stefan Uhlich, Ryoga Matsuo, Sony Europe B.V., ZNL Deutschland, DE; Andrea Bonetti, Arun Venkitaraman, Ali Momeni, Chia-Yu Hsieh, Lorenzo Servadei, SonyAI, CH; Eisaku Ohbuchi, Sony Semiconductor Solutions, JP

GRAPHDTA: FAST DYNAMIC TIMING ANALYSIS FOR CIRCUITS WITH GRAPH REPRESENTATION LEARNING

Guangxi Fan, Tianliang Ma, Xuguang Sun, Xun Wang, Leilai Shao, Shanghai Jiao Tong University, CN; Xiaolei Zhu, Zhejiang University, CN; Zhiping Yu, Tsinghua University, CN

GRAPHITRON: A DOMAIN SPECIFIC LANGUAGE FOR FPGA-BASED GRAPH PROCESSING ACCELERATOR GENERATION

Xinmiao Zhang, Zheng Feng, Shengwen Liang, Cheng Liu, Lei Zhang, Huawei Li, Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN; Xinyu Chen, Hong Kong University of Science and Technology (HKUST), Guangzhou, CN

GRL: REDESIGN DISTRIBUTED REINFORCEMENT LEARNING TRAINING ON ONE GPU

Zhikuang Xin, Zhenghong Wu, Rongqiang Cao, Haoyu Wang, Haisha Zhao, Jue Wang, Yangang Wang, University of Chinese Academy of Sciences, CN

HADA: LEVERAGING MULTI-SOURCE DATA TO TRAIN LARGE LANGUAGE MODELS FOR HARDWARE SECURITY ASSERTION GENERATION

Weimin Fu, Xiaolong Guo, Kansas State University, US; Yiting Wang, Zelin Lu, Gang Qu, Univ. of Maryland, College Park, US; Yifang Zhao, University of Science and Technology of China, CN

HEADTILE: A SCALABLE AND EFFICIENT ACCELERATOR FOR LARGE LANGUAGE MODEL INFERENCE WITH 3D MEMORY INTEGRATION

Qingshan Xue, Yihao Shi, Xueyi Zhang, Bo Wang, Shengbai Luo, Yunping Zhao, Sheng Ma, Tiejun Li, National University of Defense Technology, CN

HIGH-LEVEL ACCELERATION OF QUANTUM SIMULATION FRAMEWORKS ON RECONFIGURABLE HARDWARE

FNU Pratibha, Anshul Maurya, Naveed Mahmud, Florida Institute of Technology, US; Vinayak Jha, Ishraq Islam, Manu Chaudhary, Alvir Nobel, Kieran Egan, Esam El-Araby, The University of Kansas, US

HIVE: A HIERARCHICAL INVERSE GRAPH CONSTRUCTION FRAMEWORK FOR VERILOG CODE GENERATION AND COMPILATION ERROR CORRECTION USING LARGE LANGUAGE MODELS

Qingchen Zhai, Zhiwei Zhang, Institute of Automation, Chinese Academy of Sciences, CN; Frank Qu, University of California, Santa Barbara, CN; Hao Yu, Charles Young, Ling Liang, Tao Xie, Peking University, CN; Yuan Xie, Hong Kong University of Science and Technology (HKUST), HK

HYDRA: SOT-CAM BASED VECTOR SYMBOLIC MACRO FOR HYPERDIMENSIONAL COMPUTING

Md Mizanur Rahaman Nayan, Che-Kai Liu, Zishen Wan, Arijit Raychowdhury, Azad Naeemi, Georgia Institute of Technology, US

IM-DSE: INTELLIGENT MUTI-TARGET DESIGN SPACE EXPLORATION FOR BNN ACCELERATORS IN FPGAS

Qianyi Chen, Lu Wang, Xia Zhao, Guangda Zhang, Huadong Dai, Academy of Military Science, CN

INTELLIGENCE IN THE FENCE: CONSTRUCT A PRIVACY AND RELIABLE HARDWARE DESIGN ASSISTANT LLM

Shijie Li, Yifang Zhao, Yier Jin, University of Science and Technology of China, CN; Weimin Fu, Xiaolong Guo, Kansas State University, US

INVESTIGATING SECURITY BREACHES IN VEHICLE INFOTAINMENT SYSTEMS

Yingjie Cao, Xiapu Luo, Hong Kong Polytechnic University, CN Minrui Yan, Swinburne University of Technology, Australia; George Crane, Dean Sullivan, University of New Hampshire, US; Ya-Long Guo, 360 Security Group, CN; Haoqi Shan, Stellar Cyber, US

I-PIM: INDIRECT ADDRESS HASHING FOR EFFICIENT PROCESSING-IN-MEMORY ON GPU

Gyubeom Jeon, Jiho Kim, Jangpyo Lee, Hyojun Son, John Kim, Korea Advanced Institute of Science and Technology (KAIST), KR

LIGHTCROSS: A SECURE AND MEMORY OPTIMIZED POST-QUANTUM DIGITAL SIGNATURE CROSS

Puja Mondal, Suparna Kundu, KU Leuven, BE; Supriya Adhikary, Angshuman Karmakar, Indian Institute of Technology Kanpur, IN

LLM-BASED SOFT ERROR TOLERANT DESIGN FOR DNN ACCELERATORS

Yihao Shi, Qingshan Xue, Luo Shengbai, Tiejun Lie, Sheng Ma, National University of Defence Technology, CN

LPA-NTT: EFFICIENT LIGHTWEIGHT POLYNOMIAL MULTIPLICATION ACCELERATOR WITH HYBRID NTT ALGORITHM

Sizhao Li, Wenqi Zhang, Xing Huang, Harbin Engineering University, CN; Tiantai Deng, Kaiyuan Yang, The University of Sheffield, GB

MEMSEARCH: AN EFFICIENT MEMRISTIVE IN-MEMORY SEARCH ENGINE WITH CONFIGURABLE SIMILARITY MEASURES

Yingjie Yu, Houji Zhou, Jiancong Li, Tong Hu, Yi Li, Xiangshui Miao, Huazhong University of Science and Technology, CN; Jia Chen, The Hong Kong University of Science and Technology, HK

SUNDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

MERINDA: MODEL RECOVERY IN FPGA BASED DYNAMIC ARCHITECTURE
Bin Xu, Ayan Banerjee, Sandeep Gupta, Arizona State University, US

MITIGATING RESOURCE CONTENTION FOR RESPONSIVE ON-DEVICE MACHINE LEARNING INFERENCES
Minsung Kim, Jihoon Lee, Seongjin Chou, Whisoo Chung, Kilho Lee, Soongsil University, KR; Woosung Kang, Hoon Sung Chwa, Daegu Gyeongbuk Institute of Science and Technology, KR; Hyosu Kim, Chung-Ang University, KR; Sangeun Oh, Korea University, KR

MOOPSE: LEVERAGING HIGH-RADIX BOOTH ENCODERS FOR AREA-EFFICIENT MATRIX MULTIPLY OPERATIONS
Chenlin Shi, Hayato Yamaki, Hiroki Honda, Shinobu Miwa, The University of Electro-Communications, JP; Toru Koizumi, Nagoya Institute of Technology, JP; Ryota Shioya, The University of Tokyo, JP

MPE: A POWER-EFFICIENT EDGE-DEVICE MAMBA PROCESSOR WITH MULTI-DIMENSIONAL CALCULATION-COMPRESSION SCHEME
Zhou Wang, Anil Bharath, Manos Drakakis, Imperial College London, GB; Haochen Du, Hong Kong University of Science and Technology (HKUST), CN; Xiaonan Tang, Beijing Wisemay Science and Technology Co.,LTD, CN; Shushan Qiao, Institute of Microelectronics of Chinese Academy of Sciences, CN; Shouyi Yin, Tsinghua University, CN

MTRACE : TRUSTED LOGGING USING ARM DWT ON EMBEDDED DEVICES
Dong Kyun Yang, Jinsoo Jang, Chungnam National University, KR; Seyoung Baik, Sangwook Lee, ETRI, KR

MULTIPLE ROW BUFFER DRAM
K. Chitra, Aryabartta Sahu, Indian Institute of Technology, Guwahati, IN; Minesh Patel, Rutgers University, US, Arjun Dey, Nutanix, IN

NLS: NATURAL-LEVEL SYNTHESIS FOR HARDWARE IMPLEMENTATION THROUGH GENAI
Kaiyuan Yang, Xinyi Wang Bingjie Lu, Yanbo Wang, Charith Abhayaratne, Tiantai Deng, The University of Sheffield, GB; Huang Ouyang, Long Jin, Lanzhou University, CN; Sizhao Li, Harbin Engineering University, CN

OPENASSERT: TOWARDS OPEN-SOURCE LARGE LANGUAGE MODELS FOR ASSERTION GENERATION
Anand Menon, Samit Miftah, Amisha Srivastava, Kanad Basu, University of Texas at Dallas, US; Shamik Kundu, Arnab Raha, Souvik Kundu, Suvadeep Banerjee, Deepak Mathaikutty, Intel Labs, US

OPENGC: AN OPEN-SOURCE GAIN CELL COMPILER
Xinxin Wang, Lixian Yan, Shuhan Liu, Luke Upton, Shengman Li, H.-S. Wong, Stanford University, US; Jesse Cirimelli-Low, Matthew Guthaus, University of California, Santa Cruz, US

OPTI-SPISSL: A HIGHLY RECONFIGURABLE HARDWARE GENERATION FRAMEWORK FOR SPIKING SELF-SUPERVISED LEARNING ON HETEROGENEOUS SOC
Heuijee Yun, Daejin Park, Kyungpook National University, KR

OT-CRL: ONLINE TUNING OF DRAM CONTROLLERS USING CONTINUAL REINFORCEMENT LEARNING
Yen Hao Huang, National Tsinghua University, TW

PECA: POLYHEDRAL-BASED EFFICIENT COMPILER FOR AI APPLICATIONS ON CGRAS
Mingyang Kou, Weiqing Ji, Hailong Yao, University of Science and Technology Beijing, CN; Shouyi YIN, Tsinghua University, CN

PIANO: A MULTI-CONSTRAINT PIN ASSIGNMENT-AWARE FLOORPLANNER
Zhexuan Xu, Kexin Zhou, Jie Wang,; Zijie Geng, Feng Wu, University of Science and Technology of China, CN; Siyuan Xu, Shixiong Kai, Mingxuan Yuan, Huawei, CN

PROCAMO: A FAST POST-MANUFACTURING PROGRAMMABLE CAMOUFLAGED LOGIC FAMILY RESILIENT TO DPA ATTACK AND REVERSE ENGINEERING
Seo Hyun Kim, Jongmin Lee, Ajou University, KR; Minhyeok Jeong, Sungkyunkwan University, KR

REVEAL: REVERSE ENGINEERING OF MULTIPLIER ARCHITECTURES VIA GRAPH LEARNING FOR COMPUTER ALGEBRA VERIFICATION
Chen Chen, Cunxi Yu, University of Maryland, College Park, US; Daniela Kaufmann, TU Wien, AT; Chenhui Deng, Nvidia, US

SAFESSD: TREELESS SSD PROTECTION BY LEVERAGING PHYSICAL ADDRESS AS VERSION NUMBER
Talha Ahmed, Seokin Hong, Sungkyunkwan University, KR

SAYRAM: A HARDWARE-SOFTWARE CO-DESIGN TO ACCELERATE WIRELESS BASEBAND PROCESSING
Xinbing Zhou, Hainan University, CN; Shaobo Shi, Shaohan Liu Yunxiang Tang, Dake Liu, Ultichip Communication Technology, CN; Peng Hao, Northwestern Polytechnical University, CN; Yi Man, Beijing University of Posts and Telecommunications, CN

SCALABLE FRAMEWORK FOR TRAFFIC RULE ENFORCEMENT IN AUTONOMOUS DRIVING: EVALUATING ADAPTABILITY ACROSS EDGE PLATFORMS
Fatima Idrees, Narmada Ambigapathy, Peer Adelt, Charles Steinmetz, Achim Rettberg, Hamm-Lippstadt University of Applied Sciences, DE

SCALAR RUNAHEAD
Dean You, Xiaoxuan Wang, Yushu Du, Zhihang Tan, Hui Wang, Zhe Jiang, Southeast University, CN; Jieyu Jiang, Shuai Zhao, Sun Yat-sen University, CN; Wenbo Xu, Huazhong University of Science and Technology, CN; Jiapeng Guan, Dalian University of Technology, CN; Ran Wei, Lancaster University, GB

SCHEMATO - AN LLM FOR NETLIST-TO-SCHEMATIC CONVERSION

Ryoga Matsuo, Stefan Uhlich, Lukas Mauch, Augusto Capone, Sony Europe B.V., ZNL Deutschland, DE; Arun Venkitaraman, Andrea Bonetti, Chia-Yu Hsieh, Ali Momeni, Lorenzo Servadei, SonyAI, CH; Eisaku Ohbuchi, Sony Semiconductor Solutions, JP

SCMG: SCALABLE AND CONFIGURABLE FPGA-BASED MULTIPLIER GENERATOR USING INTEGER LINEAR PROGRAMMING

Yao Shangshang, Independent Researcher, CN; Zhu Junyi, Lang Qingjie, Wang Ruoxi, Shen Li, National University of Defense Technology, CN

SECONN: AN OPTICAL NEURAL NETWORK FRAMEWORK WITH CONCURRENT DETECTION OF THERMAL FAULT INJECTION ATTACKS

Kota Nishida, Yoshihiro Midoh, Noriyuki Miura, Jun Shiomi, Osaka University, JP; Satoshi Kawakami, Kyushu University, JP

SOFTONIC: A PHOTONIC DESIGN APPROACH TO SOFTMAX ACTIVATION FOR HIGH-SPEED ANALOG AI ACCELERATION

Priyabrata Dash, Dharanidhar Dang, The University of Texas at San Antonio, US; Anxiao Jiang, Texas A&M University, US

SOLVING MULTIDIMENSIONAL PARTIAL DIFFERENTIAL EQUATIONS ON QUANTUM HARDWARE

Manu Chaudhary, Kareem El-Araby, Alvir Nobel, Vinayak Jha, Dylan Kneidellshraq Islam, Esam El-Araby, The University of Kansas (KU), US

SPEEDING UP GLOBAL PLACEMENT METHOD BY INTEGRATING A PRECORRECTED FFT SOLVER

Hangyu Zhang, Sachin S. Sapatnekar, University of Minnesota, US

SQUEEZING OUT HIDDEN MARGINS FOR HARD-TO-SOLVED IR VIOLATIONS IN VLSI BY EXTRACTING TIMING SLACK METHODOLOGY

Yu-Wen Lin, Wei-Chih Hsieh, Florentin Dartu, TW Semiconductor Manufacturing Company, TW

SWIFTMAX: REDUCING TRAINING TIME FOR LEARNABLE SOFTMAX ALTERNATIVE IN CUSTOMIZED ACCELERATION

Haoxiang Sun, Yiqi Liu, Wenbo Zhang, Zhenshan Bao, Beijing University of Technology, CN

SYNALIGN: ANNOTATING HDLS WITH SYNTHESIS RESULTS

Sakshi Garg, Jose Renau, University of California, Santa Cruz, US

TEA-GNN: TECHNOLOGY NODE EXPLORATION ACCELERATION VIA END-OF-FLOW METRIC PREDICTION

Luis Humberto Pena Trevino, TÃ©lÃ©com Paris, FR; Lirida Naviner, Télécom Paris, FR; Fady Abouzeid, STMicroelectronics, FR

TICKTOCKSTACK: IN-DATAPATH CURRENT IMBALANCE ELIMINATION USING CLOCKED DIFFERENTIAL LOGIC IN A VOLTAGE STACKED VECTOR PROCESSOR

MichaÅ, Gorywoda, Wanyeong Jung, Korea Advanced Institute of Science & Technology (KAIST), KR

TILER: HARDWARE-IN-THE-LOOP MITIGATION OF SOFTWARE TIMING SIDE-CHANNEL VULNERABILITIES

Tasneem Suha, Prabuddha Chakraborty, University of Maine, US; Rima Awad, Oak Ridge National Laboratory, US

TSO: BOOSTING REMATERIALIZATION TRAINING VIA OPTIMAL TENSOR SCHEDULING OPTIMIZATION

Yu Tang, Lujia Yin, Linbo Qiao, Dongsheng Li, National University of Defense Technology, CN; Qiao Li, Xiamen University, CN; Cheng Li, University of Science and Technology of China, CN; Wujun Wen, Hengjie Li, Xingcheng Zhang, Shanghai Artificial Intelligence Laboratory, CN

UNARY POSITIONAL SYSTEM: FLEXIBLE BALANCE OF HARDWARE AREA AND PERFORMANCE

Zeshi Liu, Haihang You, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Science, CN; Zheng Weng, Beijing University of Posts and Telecommunications, CN

UNLEASHING THE POTENTIAL OF HYPERDIMENSIONAL COMPUTING ON SKYRMION RACETRACK MEMORIES

Yu-Pei Liang, National Chung Cheng University, TW; Jian-Yi Pan, Wei-Kuan Shih, National Tsing Hua University, TW; Yen-Ting Chen, National Taiwan University, TW; Yuan-Hao Chang, Academia Sinica, TW

UNSTRUCTURED SPARSE NEURAL NETWORK COMPRESSION BASED ON GRAPH MATCHING FOR ENERGY-EFFICIENT COMPUTE-IN-MEMORY

Teng Wan, Yongpan Liu, Huazhong Yang, Xueqing Li, Tsinghua University, CN; Yu Cao, Beijing Institute of Technology, CN

THE EVOLUTION OF INNOVATION: THE DAWN OF REASONING AGENTS IN CHIP DESIGN

Time: 8:45 AM - 10:00 AM

Topic Area(s): AI, Design

Session Type: Keynote

Room: 3007, Level 3

Description: DAC has long been a beacon for technological foresight and innovation in the semiconductor industry. As we look beyond 2025, the landscape of chip design is poised for another transformative leap with the advent of reasoning agents. This evolution builds upon the foundational milestones set by the Electronics Resurgence Initiative (ERI), which revitalized U.S. semiconductor research, and the integration of cloud computing for silicon. The emergence of Generative AI (GenAI) heralds a new era of creativity and efficiency in design processes across multiple domains.

In this keynote, we will explore how reasoning agents are set to revolutionize the semiconductor industry by offering unprecedented capabilities in problem-solving and decision-making. These agents, drawing inspiration from scientific methodologies in other domains, promise to enhance the precision and speed of design, automate manual tasks, while also fostering a collaborative environment between human designers and AI systems. We will delve into the practical applications of these agents, showcasing their potential to streamline complex design challenges, drive innovation, and increase productivity.

The DAC continues to play a crucial role in this journey, serving as a platform for sharing insights, fostering collaboration, and setting the stage for the next wave of technological advancements. By embracing the synergy between AI and human expertise, we are not only shaping the future of microelectronics but also redefining the boundaries of what is possible in chip design. Join us as we navigate this exciting frontier and explore the opportunities that lie ahead.

Speakers: William Chappell, Microsoft

ACCELERATOR PACKAGE AND SYSTEM DESIGN FOR THE AI ERA

Time: 10:15 AM - 11:00 AM

Topic Area(s): AI

Session Type: Analyst Presentation

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: This session will discuss the design of accelerator packages and systems tailored for the AI era, addressing the need for improved performance, scalability, and energy efficiency to support complex AI workloads.

Speaker: Dylan Patel, SemiAnalysis, US

TAMING THE WAVEFORM TSUNAMI: AGENTIC AI FOR SMARTER DEBUGGING

Time: 10:30 AM - 11:00 AM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Modern chip design verification generates massive waveform dumps—often terabytes in size—making it nearly impossible for engineers to manually debug and trace root causes efficiently. Traditional waveform viewers and rule-based scripts fall short when faced with the scale, complexity, and subtlety of today's RTL designs. In this Exhibitor Forum session, we introduce ChipAgents, an agentic AI system purpose-built to tackle waveform analysis at scale. By combining structured reasoning, semantic search, and interactive agents, ChipAgents empowers verification engineers to ask natural-language questions, trace failure propagation across time and modules, and receive contextualized explanations grounded in the RTL and waveform data.

Our approach moves beyond static signal inspection. Agents dynamically explore the design hierarchy, generate hypotheses, and interpret causality—turning waveform dumps into actionable insights. Whether you're facing race conditions, signal glitches, or protocol violations, our system helps you find the needle in the haystack—faster and more reliably than ever before.

We'll showcase real-world case studies where ChipAgents successfully identified root causes in minutes—debugs that previously took days. The demo includes multi-agent workflows that collaborate across testbench logs, waveform traces, and RTL to deliver end-to-end failure analysis.

This talk will appeal to EDA tool developers, DV engineers, and design leads seeking scalable, AI-powered solutions for debugging in the era of increasingly complex SoCs. Join us to see how agentic AI is redefining RTL understanding—one waveform at a time.

Speakers: Zackary Glazewski, William Wang, ChipAgents.ai, US

CDC-RDC INTER-OPERABLE COLLATERAL STANDARDIZATION

Time: 10:30 AM - 12:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2012, Level 2

Description: CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOC's having 2 trillion+ transistors and chiplets having 7+ SOC's. Today CDC verification has become a multifaceted effort across the chips designed for clients, servers, mobile, automotives, memory, AI/ML, FPGA etc... with focus on cleaning up of thousands of clocks and constraints, integrating the SVA's for constraints in validation environment to check for correctness, looking for power domain and DFT logic induced crossings, finally signing off with netlist CDC to unearth any glitches and corrupted synchronizers during synthesis.

As the design sizes increased in every generation, the EDA tools could not handle running flatly and the only way of handling design complexity was through hierarchical CDC-RDC analysis consuming abstracts. Also, hierarchical analysis helps to enable the analysis in parallel with teams across the globe. Even with all these significant progress in capabilities of EDA tools the major bottleneck in CDC-RDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools. Different vendor tool abstracts are seen because of multiple IP vendors, even in house teams might deliver abstracts generated with different vendors tools.

The Accellera CDC Working-Group aims to define a standard CDC-RDC IP-XACT / TCL model to be portable and reusable regardless of the involved verification tool.

As moving from monolithic designs to IP/SOC with IPs sourced from a small/select providers to sourcing IPs globally (to create differentiated products), the quality must be maintained as driving faster time-to-market. In areas where the standards (SystemVerilog, OVM/UVM, LP/UPF) are present, the integration is able to meet the above (quality, speed). However, in areas where standards (in this case, CDC-RDC) are not available, most options trade-off either quality, or time-to-market, or both. Creating a standard for inter-operable collateral addresses this gap.

This special session aims to remind the definitions of CDC-RDC Basic Concepts and constraints, as well as the description of the reference verification flow, and addressing the goals, scope, structure & deliverables of the Accellera CDC Working Group in order to elaborate a specification of the standard abstract model.

Moderators: Iredamola Olopade, Intel Corporation, US

Speakers: Anupam Bakshi, Agnisys Inc., US; Bill Gascoyne, Blue Pearl Software, US; Chetan Choppali Sudarshan, Marvell, US; Don Mills, Microchip Technology INC, US; Farhard Ahmed, Siemens, US

NEXT GENERATION UCIE: ENABLING A THRIVING OPEN CHIPLET ECOSYSTEM

Time: 10:30 AM - 12:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2008, Level 2

Description: The promise of an open industry standard that offers high-bandwidth, low-latency, power-efficient, cost-effective on-package connectivity between chiplets continues to evolve at blazing speed. Ever since UCIe – or Universal Chiplet Interconnect Express 1.0 was first released in March 2022, it has seen significant industry adoption. Version 1.0 was followed by Version 1.1 (Released August 2023) with key features such as runtime health monitoring for automotive and high-reliability applications. Recently, in August 2024, the latest standard, 2.0 was released.

This session aims to cover the evolution, usage and impact of UCIe through 3 different sessions: First, Dr. Das Sharma, Chair of UCIe Consortium, will provide the overview, evolution and future of UCIe. Then Dr. Zorian will delve into details of one of the key modules in UCIe: health monitoring. Finally, Mr. Jani will cover how customer usage is both benefiting from existing standards as well as driving new versions of the standard itself, highlighting its significant advancements in System-in-Package (SiP) design and paving the way for high-density systems with improved performance and reduced power consumption.

Organizer(s): Sashi Obilisetty, Synopsys, US

Moderators: Rakesh Kinger, Google

Speakers: Debendra Das Sharma, Intel Corporation, US; Yervant Zorian, Synopsys, US; Dharmesh Jani, Meta, US

SURVIVING MONTE CARLO – CIRCUIT OPTIMIZATION IDEAS

Time: 10:30 AM - 12:00 PM

Topic Area(s): IP

Session Type: Engineering Track

Room: 2010, Level 2

Description: Analog circuits are difficult to optimize and traditionally require a large number of Spice level simulations to determine performance and sensitivities. This session presents new ideas that employ AI or other methods to facilitate this task.

- **Accelerating SRAM Design Cycles With Additive AI Technology**
  Mohamed Atoua, Ajaj Ansari, Siemens, IN; Sriharsha Enjapuri, MediaTek, IN
- **Novel TRNG Verification with a High-Performance Simulation Methodology**
  Ting-Yen Chiang, Microsoft, US; Shravan Ramesh, Lih-Jen Hou, Siemens, US
- **Accelerating Bandgap Reference High-Sigma Verification with Additive AI Technology**
  Barry Thompson, Lawrence Prather, Microsoft, US; Mohamed Atoua, Hadar Baran, Kevin Krieger, Siemens, CA
- **AI-Driven Multi-Parameters Multi-Objectives Optimization Flow For High-Speed Transmission Line In SerDes Design**
  Long Qin, JinRong Yan, Dengjie Wang, Hang Sun, Xuewei Ding, Sanechips Technology Co., Ltd., CN; Xiaomei You, Rodger Luo, Jie Cheng, Ansys, CN
- **Statistical Analysis using AI-ML Enabled SPICE Solution to Get Tail Samples for High Linearity Delta Sigma Converters**
  Vaibhav Garg, Sanyam Jain, Atul Bhargava, Ankur Bal, Anil Dwivedi, STMicroelectronics, IN; Prayes Jain, Cadence Design Systems, Inc., IN
- **Advanced Verification Solutions for Communication ICs to Ensure High Quality Amid PVT Variations**
  Tomohiro Ishida, Shunichi Kobo, THine Electronics, JP; Yuling Lin, Lih-Jen Hou, Siemens, US

Session Chair(s): Navid Farazmand, Intel

ALL QUIET ON THE PROCESSOR FRONT: NEXT-GEN PROCESSOR SECURITY AND ENCLAVE INNOVATIONS

Time: 10:30 AM - 12:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3008, Level 3

Description: As computing systems become increasingly complex, securing CPUs and enclave-based architectures remains a top priority. This hardware security session showcases cutting-edge research on security primitives and architectural enhancements for these critical systems. The selected papers explore fuzzing-based techniques for identifying critical CPU vulnerabilities, propose practical solutions for secure virtual machine architectures, analyze security assets in System-on-Chip (SoC) designs, and extend TrustZone technology to heterogeneous FPGA architectures.

- **IntraFuzz: Coverage-Guided Intra-Enclave Fuzzing for Intel SGX Applications**
  Jinhua Cui, Qiao Peng, Yiwen Yao, Ke Ye, Jiliang Zhang, Hunan University, CN
- **BPUFuzzer: Effective Fuzz Testing for Branching Transient Execution Vulnerabilities of RISC-V CPU**
  Rihui Sun, Jin Wu, Hanyin Liu, Zikang Tao, Jian Dong, Harbin Institute of Technology, CN; Gang Qu, University of Maryland, College Park, US; Dongsheng Wang, Yongqiang Lyu, Tsinghua University, CN
- **ADVeRL-ELF: ADVersarial ELF Malware Generation using Reinforcement Learning**
  Akshara Ravi, Vivek Chaturvedi, Indian Institute of Technology, Palakkad, IN; Muhammad Shafique, New York University, Abu, AE
- **Identifying System-on-Chip Security Assets with Structure-Based Analysis**
  Wei-Kai Liu, Duke University, US; Benjamin Tan, University of Calgary, CA; Krishnendu Chakrabarty, Arizona State University, US
- **Zion: A Practical Confidential Virtual Machine Architecture on Commodity RISC-V Processors**
  Jie Wang, Juan Wang, Wuhan University, CN; Yinqian Zhang, SUSTech, CN
- **FPGA-TrustZone: Security Extension of TrustZone to FPGA for SoC-FPGA Heterogeneous Architecture**
  Shupeng Wang, Fan Xindong, Xiao Xu, Shuchen Wang, Lei Ju, Zimeng Zhou, Shandong University, CN

Session Chair(s): Samuel Pagliarini, Carnegie Mellon University; Gang Qu, University of Maryland

BALANCING SPEED AND MEMORY: ADVANCING LLM ACCELERATION

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: As LLMs grow in scale, optimizing both memory usage and computational throughput becomes essential. This session introduces six interesting approaches to overcoming key bottlenecks in LLM and MoE inference, including semantic-aware KV cache compression, outlier-free quantization for FPGA acceleration, and hybrid CPU-GPU execution strategies. Additionally, new techniques in sparse attention balancing, FPGA overlays for state-space models, and fusion-aware workload optimization enable more efficient processing. These works comes as a timely effort to inspire next-generation AI accelerators that achieve higher performance while maintaining resource efficiency.

- **MambaOPU: An FPGA Overlay Processor for State-Space-Duality-Based Mamba Models**
  Shaoqiang Lu, Shanghai Jiao Tong University, Shanghai, CN; Xuliang Yu, Xinsong Sheng, Liang Zhao, Zhejiang University, CN; Tiandong Zhao, Siyuan Miao, Lei He, University of California, Los Angeles, US; Chen Wu, TingJung Lin, Ningbo Institute of Digital Twin, Eastern Institute of Technology, Ningbo, CN, CN
- **A Cross-model Fusion-Aware Framework for Optimizing (gather-matmul-scatter)s Workload**
  Yaoxiu Lian, Zhihong Gou, Yibo Han, Jiaming Xu, Ningyi Xu, Guohao Dai, Shanghai Jiao Tong University, CN; Zhongming Yu, University of California, San Diego, US; Sheng Yuan, Zhilin Pei, Xingcheng Zhang, Shanghai Artificial Intelligence Laboratory, CN
- **HybriMoE: Hybrid CPU-GPU Scheduling and Cache Management for Efficient MoE Inference**
  Shuzhang Zhong, Ling Liang, Runsheng Wang, Ru Huang, Meng Li, Peking University, CN; Yanfan Sun, Beihang University, CN
- **ClusterKV: Manipulating LLM KV Cache in Semantic Space for Recallable Compression**
  Guangda Liu, Chengwei Li, Jieru Zhao, Chenqi Zhang, Minyi Guo, Shanghai Jiao Tong University, CN
- **DuoQ: A DSP Utilization-aware and Outlier-free Quantization for FPGA-based LLMs Acceleration**
  Zhuoquan Yu, Huidong Ji, Yue Cao, Junfu Wu, Xiaoze Yan, Lirong Zheng, Zhuo Zou, Fudan University, CN
- **Libra: A Hybrid-Sparse Attention Accelerator Featuring Multi-Level Workload Balance**
  Faxian Sun, Runzhou Zhang, Zhenyu Liu, Heng Liao, Zhinan Qin, Jianli Chen, Jun Yu, Kun Wang, Fudan University, CN

Session Chair(s): Chaojian Li, Georgia Institute of Technology; Zhongzhi Yu , Nvidia

BREAKING BOUNDARIES IN ACCELERATOR DESIGN: PHOTONIC, TIME-DOMAIN, AND SECURITY-DRIVEN AI

Time: 10:30 AM - 12:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: AI acceleration is evolving beyond conventional silicon, embracing photonic, time-domain, and security-enhanced architectures. This session showcases breakthroughs in high-speed photonic tensor cores, nonlinear time-domain processing, FeFET-based security solutions, and specialized AI accelerators for LLMs and combinatorial optimization. By leveraging novel computing paradigms, these innovations push the boundaries of performance, efficiency, and security in AI hardware design.

- **UniCAIM: A Unified CAM/CIM Architecture with Static-Dynamic KV Cache Pruning for Efficient Long-Context LLM Inference**
  Weikai Xu, Wenxuan Zeng, Qianqian Huang, Peking University, CN; Meng Li, Ru Huang, Peking University, CN
- **P-DAC: Power-Efficient Photonic Accelerators for LLM Inference**
  Wen-Tse Chang, Chun-Feng Wu, National Yang Ming Chiao Tung University, TW; Yun-Chen Lo, Harvard University, US
- **A PulseWidth-IN-PulseWidth-Out Universal Nonlinear Processing Element for Time-Domain In-Memory Computing Systems**
  Yihao Chen, Pengcheng Feng, Zhigang Li, Gang Chen, Xianghua Lu, Rongxuan Shen, Xiaoxin Xu, Institute of Semiconductors Chinese Academy of Sciences, CN
- **PUFiM: A Robust and Efficient FeFET-Based Security Solution Merging Physical Unclonable Function with Compute-in-Memory for Edge AI**
  Taixin Li, Jianfeng Wang, Huazhong Yang, Xueqing Li, Tsinghua University, CN; Thomas Kämpfe, Fraunhofer IPMS, DE; Kai Ni, University of Notre Dame, US; Vijaykrishnan Narayanan, Pennsylvania State University, US
- **TAXI: Traveling Salesman Problem Accelerator with X-bar-based Ising Macros Powered by SOT-MRAMs and Hierarchical Clustering**
  Sangmin Yoo, Francesca Iacopi, Dwaipayan Biswas, James Myers, imec, BE; Amod Holla, Sourav Sanyal, Dong Eun Kim, Kaushik Roy, Purdue University, US
- **A Mixed-Signal Photonic SRAM-based High-Speed Energy-Efficient Photonic Tensor Core with Novel Electro-Optic ADC**
  Md Abdullah-Al Kaiser, Akhilesh Jaiswal, University of Wisconsin, Madison, US; Sugeet Sunder, Ajey Jacob, University of Southern California, US

Session Chair(s): Yu Cao, University of Minnesota

BREAKTHROUGHS IN TIMING PREDICTION, ANALYSIS, AND OPTIMIZATION

Time: 10:30 AM - 12:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: This session provides insights into innovative methodologies addressing key challenges in timing analysis, prediction, and optimization. Topics include ultra-fast statistical static timing analysis, machine learning-driven timing prediction, and advanced characterization techniques. Additionally, the session explores a fast clock skew scheduling algorithm for improved timing and an approach to mitigating security risks posed by glitch-induced transitions in cryptographic hardware.

- **INSTA: An Ultra-Fast, Differentiable, Statistical Static Timing Analysis Engine for Industrial Physical Design Applications**
  Yi-Chen Lu, Kishor Kunal, Rongjian Liang, Haoxing Ren, Nvidia, US; Zizheng Guo, Peking University, CN
- **GTN-Path: Efficient Path Timing Prediction through Waveform Propagation with Graph Transformer**
  Lihao Liu, Beisi Lu, Yunhui Li, Li Shang, Fan Yang, Fudan University, CN
- **Generative Model Based Standard Cell Timing Library Characterization**
  Hao-Yu Wu, Hsin-Tzu Chang, Shiuan-Yun Ding, Iris Hui-Ru Jiang, National Taiwan University, TW; Benson Tsao, Vinson Wu, Wei-Kai Shih, Synopsys, TW
- **Truly Pre-Routing Timing Prediction via Considering Power Delivery Networks**
  Yuyang Ye, Tinghuan Chen, The Chinese University of Hong Kong, Shenzhen, CN; Mingwei He, Lizheng Ren, Jun Yang, Southeast University, CN; Longxing Shi, Southeast University, CN; Jianwang Zhai, Beijing University of Posts and Telecommunications, CN
- **A Fast, Iterative Clock Skew Scheduling Algorithm with Dynamic Sequential Graph Extraction**
  Shijian Chen, Biwei Xie, Mingyu Chen, State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, CN; Yihang Qiu, University of Chinese Academy of Sciences, CN; Xingquan Li, Peng Cheng Laboratory, CN
- **GLiTCH : GLiTCH induced Transitions for Secure Crypto-Hardware**
  C.Rohin Menon, Jayanth Balasubramanian, Akshay E, Annapurna Valiveti, Chester Rebeiro, Janakiraman Viraraghavan, Indian Institute of Technology, Madras, IN

Session Chair(s): Zhiyao Xie, HKUST; Xin Zhao, IBM

CIRCUIT BREAKERS: SECRETS UNLEASHED!

Time: 10:30 AM - 12:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3003, Level 3

Description: In today's integrated circuits, security threats lurk beneath the surface, waiting to be uncovered. This DAC session presents groundbreaking research exposing vulnerabilities in ARM-FPGA SoCs and AMD Zen processors. Presentations in this session provide deep insights to the exploits of on-chip sensors, last-level cache side channels, and the integrity of innovative technologies including zero-knowledge proofs, approximate neural networks, and quantum circuits. This session will also explore vital countermeasures to strengthen designs against emerging threats. Join us in this essential dialogue on securing circuits for the future — let's break the silence together!

- **AmpereBleed: Exploiting On-chip Current Sensors for Circuit-Free Attacks on ARM-FPGA SoCs**
  Xin Zhang, Yi Yang, Jiajun Zou, Qingni Shen, Peking University, CN; Zhi Zhang, Yansong Gao, University of Western Australia, AU; Zhonghai Wu, Peking University, CN; Trevor E. Carlson, National University of Singapore, SG
- **ZenLeak: Practical Last-Level Cache Side-Channel Attacks on AMD Zen Processors**
  Han Wang, Ming Tang, Quancheng Wang, Ke Xu, Wuhan University, CN; Yinqian Zhang, Southern University of Science and Technology, CN
- **ZK-Hammer: Leaking Secrets from Zero-Knowledge Proofs via Rowhammer**
  Junkai Liang, Xin Zhang, Daqi Hu, Qingni Shen, Yuejian Fang, Zhonghai Wu, Peking University, CN
- **Cross-Attention for AES Mode Variation in Side-Channel Analysis**
  Fanliang Hu, Nanjing University of Information Science and Technology, CN; Jian Shen, Haoyu Ma, Zhejiang Sci-Tech University, CN; Qingming Jonathan Wu, University of Windsor, CA
- **Security of Approximate Neural Networks Against Power Side-Channel Attack**
  Japa Aditya, Jack Miskelly, Maire O'Neill, Chongyan Gu, Queen's University Belfast, GB
- **TetrisLock: Quantum Circuit Split Compilation with Interlocking Patterns**
  Qian Wang, Jayden John, Ben Dong, University of California, Merced, US; Yuntao Liu, Lehigh University, US

Session Chair(s): Prabuddha Chakraborty, University of Maine

GRAPHS & TOPOLOGY: THE NEW FRONTIER IN AI MODELING

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session explores the use of graph-based and topological models in machine learning applications. It includes papers on scalable graph neural networks, the application of graph-based analysis for circuit stability, and innovative topology representation for layout pattern detection. These papers push the boundaries of leveraging graph-based models for complex real-world problems in machine learning.

- **Towards Training Robustness Against Dynamic Errors in Quantum Machine Learning**
  Shijin Duan, Xiaolin Xu, Northeastern University, US; Gaowen Liu, Charles Fleming, Ramana Kompella, Cisco, US; Shaolei Ren, University of California, Riverside, US
- **CirSTAG: Circuit Stability Analysis on Graph-Based Manifolds**
  Wuxinlin Cheng, Yihang Yuan, Zhuo Feng, Stevens Institute of Technology, US; Chenhui Deng, Nvidia, US; Ali Aghdaei, University of California, San Diego, US; Zhiru Zhang, Cornell University, US
- **ParGNN: A Scalable Graph Neural Network Training Framework on multi-GPUs**
  Junyu Gu, Shunde Li, Rongqiang Cao, Jue Wang, Zijian Wang, Zhiqiang Liang, Fang Liu, Chunbao Zhou, Yangang Wang, Xuebin Chi, University of Chinese Academy of Sciences, CN; Shigang Li, Beijing University of Posts and Telecommunications, CN
- **Delving into Topology Representation for Layout Pattern: A Novel Contrastive Learning Framework for Hotspot Detection**
  Silin Chen, Kangjian Di, Li Du, Ningmu Zou, Nanjing University, CN; Guohao Wang, Wenzheng Zhao, ZetaTech Co., Ltd., CN
- **SuperFast: Fast Supernet Training using Initial Knowledge**
  Moritz Thoma, Shambhavi Balamuthu Sampath, Nael Fasfous, Alexander Frickenstein, Manoj Rohit Vemparala, BMW AG, DE; Emad Aghajanzadeh, University of Hamburg, DE; Pierpaolo Mori, Politecnico di Torino, IT; Daniel Mueller-Gritschneder, TU Wien, AT; Ulf Schlichtmann, Technical University of Munich, DE
- **LA-MTL: Latency-Aware Automated Multi-Task Learning**
  Shambhavi Balamuthu Sampath, Moritz Thoma, Lukas Frickenstein, Nael Fasfous, Manoj Rohit Vemparala, Alexander Frickenstein, BMW, DE; Sami Sawani, Technical Ulf Schlichtmann, Walter Stechele, Technical University of Munich, DE; Pierpaolo Mori, Passerone, Politecnico di Torino, IT

Session Chair(s): Yiting Liu, University of California, San Diego; Sercan Aygun, University of Louisiana

LLM/DL DRIVEN ANALOG CIRCUIT DESIGN AND ANALYSIS

Time: 10:30 AM - 12:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3006, Level 3

Description: Modern analog IC design faces challenges like increasing complexity, optimization, PVT variations, and simulation bottlenecks. Traditional methods struggle with large design spaces and reliability. LLMs and deep learning technologies address these issues by automating tasks, managing PVT variations, and reducing simulation costs. This session will cover the topics reinforcement learning for variation-aware designs, transfer learning for system-level optimization, universal neural simulators, GPU-accelerated passivity enforcement, and image-graph fusion for IR drop prediction, demonstrating AI's role in optimizing and enhancing analog IC design.

- **GLOVA: Global and Local Variation-Aware Analog Circuit Design with Risk-Sensitive Reinforcement Learning**
  Dongjun Kim, Junwoo Park, Chaehyeon Shin, Jaeheon Jung, Jongsun Park, Korea University, KR; Kyungho Shin, Seungheon Baek, Sanghyuk Heo, Woongrae Kim, Inchul Jeong, Joohwan Cho, SK hynix, KR
- **Graph-Guided Transfer Learning to Boost the Efficiency of System-Level Optimization of Analog/ Mixed-Signal Circuits**
  Jiaqi Wang, Georges Gielen, KU Leuven, BE
- **INSIGHT: A Universal Neural Simulator Framework for Analog Circuits with Autoregressive Transformers**
  Souradip Poddar, Yao Lai, Hanqing Zhu, David Z. Pan, University of Texas at Austin, US; Youngmin Oh, Bosun Hwang, Samsung, KR
- **G-SpNN: GPU-Accelerated Passivity Enforcement for S-Parameter Modeling with Neural Networks**
  Lijie Zeng, Jiatai Sun, Zhou Jin, University of Petroleum, Beijing, CN; Xiao Wu, Empyrean Software, CN; Dan Niu, Southeast University, CN; Tianshi Wang, University of California, Berkeley, US; Yibo Lin, Peking University, CN; Zuochang Ye, Tsinghua University, CN
- **A Novel Image-Graph Heterogeneous Fusion Framework for Static IR Drop Prediction**
  Dan Niu, Dekang Zhang, Yichao Cao, Chao Wang, Yichao Dong, Southeast University, CN; Zhou Jin, University of Petroleum-Beijing, CN; Changyin Sun, Anhui University, CN

Session Chair(s): Markus Olbrich, Leibniz University Hannover

NAVIGATING THE TIDES OF FUNDING FOR CHIPS AND SYSTEM DESIGN

Time: 10:30 AM - 12:00 PM

Topic Area(s): Design

Session Type: Research Panel

Room: 3012, Level 3

Description: From chips to systems, design and design automation are embracing extraordinary opportunities, propelled by myriad of exciting advances including (i) emerging technologies such as beyond-CMOS devices and 3D heterogeneous integration, (ii) alternative computation paradigms such as in/near-memory computing and domain-specific computing, and (iii) innovative computational methods such as large language models. At the same time, the field faces significant challenges, spurred by demanding applications like AI, autonomous systems, quantum computing and healthcare. Compounding these challenges is a growing workforce gap, which underscores the urgent need to attract and cultivate talent across the design and design automation community, spanning from chips to complete systems.

In response to these opportunities and challenges, governments and industry across the globe are making substantial investments in research and workforce development in this field. However, navigating the complexities of various funding programs for research and workforce development can be daunting even for seasoned researchers and educators. This panel brings together representatives from government funding agencies as well as academia to share their perspectives on these critical issues. Some questions to be discussed include (i) what the existing representative funding opportunities are and what specific aims that these opportunities try to address, (ii)

whether the funding opportunities have covered the needs well, and if not, what other areas would need more funding, and (iii) what common fallacies and pitfalls to avoid when preparing successful proposals.

Organizer(s): X. Sharon Hu, University of Notre Dame; Norbert When, RPTU Kaiserslautern

Moderator: R. Iris Bahar, Colorado School of Mines, US

Speakers: Tim Cheng, Hong Kong University of Science and Technology (HKUST), HK; Bastian Mohr, DFG, German Research Foundation, DE; Ian O'Connor, Lyon Institute of Nanotechnology, FR; Vivek Prasad, Natcast, US

LARGE LANGUAGE MODEL - THE "CURRENT BIG THING" IN THE SEMICONDUCTOR WORLD

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: Structural testing has been very successful in the VLSI manufacturing process to screen out faulty devices and provide high outgoing product quality. However, recent reported data from Google and Meta show that faulty chips are escaping the test programs and ending in causing serious trouble in field; e.g., Silent Data Corruptions (SDC). Meta recently reported at International Test Conference 2024 that approximately 78% of in field interruptions are attributed to confirmed hardware issues such faulty GPUs, faulty memories, etc. This calls for immediate improvements of used fault models and test patterns at manufacturing test.

This session addresses the limitations of existing fault models and test generation, and highlights further direction for better fault modelling; both for logic and memory. The first talk shows the limitations of (commercial) existing solutions. For example, reliance on the stuck-at fault model persists even though data extracted from the test literature reveals that the percentage of defects that exhibit stuck-at fault behaviour has significantly reduced over the years; real data measurements will be provided to support statement. The second talk shows how increasing random process variations in advanced low-nanometer nodes are introducing timing marginalities that can cause unpredictable failures under adverse operating conditions; such marginalities are not considered during test generation for structural manufacturing tests yet. Consequently it is not detected by currently used industrial test programs leading to a significant number of test escapes. The third talk presents Device-Aware-Test; a new approach that aims at closing the gap between fault models and real defects. The approach is demonstrated on an industrial STT-MRAM design.

- **LLMs: A Driving Force in Next Generation Digital Design Automation**
  Matheus Moreira, Meta, US
- **Generative AI: A transformational technology for IC Design**
  Serge Leef, Microsoft, US
- **LLMs Meet Post-Silicon Test Engineering: A New Era**
  Li-C. Wang, UCSB, US

Organizer(s): Sabya Das, Synopsys, US

THE GENERATIVE AI REVOLUTION IN SEMICONDUCTOR DEVELOPMENT

Time: 11:15 AM - 11:45 AM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: AI is poised to transform our world just like the Internet did. Generative AI will dramatically improve chip design efficiency and productivity, addressing the semiconductor workforce gap as chip demand rises. Discover Microsoft's vision for generative AI-driven solutions in revolutionizing semiconductor development through new efficiencies, next-gen tools, and a transformative designer experience.

Speakers: Prashant Varshney; Richard Paw, Microsoft, US

UNLOCKING THE POWER OF AI IN EDA

Time: 11:15 AM - 12:00 PM

Topic Area(s): AI, EDA

Session Type: TechTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The semiconductor industry is experiencing unprecedented growth, and this growth comes with significant challenges—more design starts, rising design complexities, shorter time-to-market, and a shrinking talent pool. To address these challenges, semiconductor companies are turning to AI-powered EDA solutions. While mainstream AI & GenAI technologies have seen rapid consumer adoption, adapting these AI technologies for EDA use cases is not straightforward due to stringent quality requirements for semiconductor design.

Ideally, EDA AI solutions that provide productivity boosts to chip designers and engineers should (a) seamlessly analyze design and verification data, (b) optimize complex processes, and (c) generate better designs. Across these functional areas, we will discuss illustrative ML, GenAI, and Agentic approaches. Additionally, we will also discuss the challenges associated with AI adoption, including data availability, model interpretability, and computational demands.

Further, we will discuss the grand vision of having a purpose-built centralized EDA AI platform. Such a platform framework can be very powerful by combining sophisticated foundational models or even IC domain-specific foundational models with a multimodal data lake to bring GenAI capabilities to push the boundaries of semiconductor innovation, paving the way for more efficient, scalable, and intelligent design processes.

Join us to explore the capabilities of EDA AI and see what the future holds!

Speakers: Amit Gupta, Siemens, CA; Dr. John Linford, Nvidia

BEYOND BREAKING THE BOTTLENECK: SMART VERIFICATION FOR MODERN COMPLEXITY

Time: 12:00 PM - 12:30 PM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Verification is increasingly becoming the defining constraint in semiconductor design, as complexity surges across software-defined architectures, massive 3D IC and chiplet-based designs, and exploding security and safety-critical requirements. Traditional approaches—relying on large regression suites, manual coverage analysis, and isolated debug—are struggling to keep up. This session explores how scalable, intelligent verification strategies are addressing these challenges through connected workflows, AI-enhanced automation, and data-driven insights. We'll discuss how to shift from reactive debugging to proactive verification planning, and how to improve engineering throughput without scaling teams or compute linearly. Real-world examples will illustrate how teams are reducing debug effort, accelerating coverage closure, and unlocking new levels of productivity. Attendees will leave with practical ideas for building smarter verification flows that are engineered for modern complexity—not just more speed, but better focus resulting in improved productivity.

Speaker: Abhi Kolpekwar, Siemens

AI'S GROWING DEMANDS: HOW ARTIFICIAL INTELLIGENCE IS REDEFINING SEMICONDUCTOR INNOVATION

Time: 1:00 PM - 1:45 PM

Topic Area(s): AI

Session Type: SKYTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The rapid evolution of artificial intelligence is fundamentally reshaping the semiconductor industry. AI workloads demand unprecedented computational power. At the same time, the explosive growth of AI inference is driving energy demands to new heights, forcing the industry to rethink power efficiency at every level – from silicon design to data-center scale optimization. This talk will explore how the demands of AI are reshaping semiconductor innovation, the balance between performance and efficiency, and the advancements that are needed in silicon engineering to power this new era of computing.

Speaker: Jeff Wittich, Ampere Computing, US

ENABLING MULTI-DIE 3DIC DESIGNS WITH AI-POWERED ECOSYSTEM COLLABORATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2008, Level 2

Description: As chip complexity grows, multi-die 3DIC designs are becoming a pivotal solution to meet performance and efficiency demands. This talk explores how ecosystem collaboration—spanning EDA tools, IP providers, and foundries—is leveraging AI to tackle the challenges of integration, thermal management, and design verification. Highlighting case studies, it demonstrates how AI-driven automation transforms traditionally siloed workflows into cohesive, scalable solutions, enabling faster time-to-market and innovative system designs. Attendees will gain insights into practical strategies for harnessing ecosystem synergies to address the growing demands of heterogeneous integration.

Organizer(s): Tanuja Rao, Synopsys, US; Pawini Mahajan, Synopsys, US

Moderator: Tanuja Rao, Synopsys, US

Speakers: Lalitha Immaneni, Intel Corporation, US; Imran Yusuf, Arm, US; Kevin Yee, Samsung, US

GRID RESILIENCE - POWERING SOLUTIONS DESIGN AND DELIVERY FOR THE PERFORMANCE PROMISES

Time: 1:30 PM - 3:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2012, Level 2

Description: Power keeps the engine humming and delivering promised performance. Learn from others that have modeled power delivery early to signoff and doing it smart - Multi-die to ML driven with an eye for analytical speed is the focus of this session.

- **IR Drop-Aware PDN Design Methodology for HBM Proxy Package Si-Interposer with 3D-IC Platform**
  Youngho Seo, Gwonhyuk Kang, Sangwon LeeKun Joo, Donghwi Won, Juhwan Lee, Jinwon Kim, Jungyun Choi, Youngsoo Sohn, Samsung, KR
- **Guided Vectorless with Multi Vector Profiling for Memory PDN Convergence**
  Alina Sebastian, Mohammed Hafiz, Google, IN
- **Machine Learning Based Dynamic IR Hotspot Estimation for SoC Designs**
  Prateek Pendyala, Jingwei Zhang, T Govindaswamy Rahul Sai, Google, US
- **Cost and Compute-Efficient IR Drop Hierarchical Signoff for Subsystem Designs**
  Varun Sharma, Arian Fanaian, Qualcomm, US; Ayush Sood, Vineela Gedela, Ansys, US
- **Comprehensive Power Integrity Analysis of a Super Large Scale 2.5DIC with Multi Silicon Bridges Embedded in Organic Interposer**
  Ping Ding, Guohua Zhou, Shineng Ma, Sanechips Technology Co., Ltd, CN; Li Zou, ShuQiang Zhang, Ansys, CN
- **Generative-AI Technology for Block and SoC IR Closure: Root-Cause and Repair Strategies**
  Jaikishan Gopal, Siki Yang, Shane Gallagher, Sandhya Karanam, Keith Tunstall, Rohit Somwanshi, Jinal Apte, Analog Devices, Inc. (ADI), US

Session Chair(s): Badhri Uppiliappan, BAE Systems, Inc.

NOVEL EDDIES IN THE IMPLEMENTATION FLOW

Time: 1:30 PM - 3:00 PM

Topic Area(s): IP

Session Type: Engineering Track

Room: 2010, Level 2

Description: A consistent and streamlined implementation flow is key for combining IP blocks into a working SoC and ensuring correct operation. This session presents new approaches for timing closure, meso-synchronous clock domains, high level synthesis, modeling of clocks and reset, randomizing memory content and managing large sets of simulation jobs.

- **Cross-Die Timing Methodology for Next-Gen Chiplet SOCs - A Shift-Left Solution for Cross-Foundry 3DIC-STA Signoff**
  Deepon Saha, Animesh Sharma, Animesh Jain, Aniket Waghide, Dhruvin Shah, Rajesh Anand, AMD, IN
- **A Completely Digital, Low-Power, and Low-Area Phase Synchronization Architecture for Meso-Synchronous Clock Domains Supporting Dynamic Frequency Scaling**
  Anurag Choudhury, Aniruddha N, Abhishek Verma, Abhinav Parashar, Texas Instruments, IN; Robin Hoel, Texas Instruments, NO
- **Optimized Digital Design Flow for Embedded Sensor Applications Using High Level Synthesis**
  Marco Castellano, Ugo Garozzo, STMicroelectronics, IT
- **Novel Clocks and Resets Architecture Model**
  Preetika Tandon, Stephen Wang, Mike Garrett, Nvidia, US
- **A Novel Approach to Generate Random/Constrained Non-Volatile-Memory Content in a UVM Environment**
  Davide Sanalitro, STMicroelectronics, IT
- **AI-Aided Flow for Digital Verification of a Multiprotocol SerDes PHY**
  Celso Figueiredo, Domingos Terra, Synopsys, PT

Session Chair(s): Shankar Hemmady, Micron Technology

BUILDING PILLARS OF QUANTUM CIRCUITS: SYNTHESIS, SIMULATION & COMPILATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3003, Level 3

Description: This discussion session discusses new research contributions in quantum computing synthesis, quantum compilation, quantum circuit simulation, and novel tool development. The first paper proposes a novel approach combining ZX-Calculus, circuit partitioning, and circuit synthesis for pulse generation in quantum circuits. Quantum layout synthesis (QLS) is a critical step in quantum program compilation; the second paper introduces a benchmark with a known optimal SWAP count that will work as an evaluation framework and a tool for advancing QLS research. Graph state is a highly entangled quantum state and is a critical resource; therefore, the third paper proposes a novel compilation framework for emitter-photonic graph state generation, leveraging a divide-and-conquer strategy. The fourth paper proposes a highly effective compilation framework that primarily operates at the high-level Pauli-based intermediate representation (IR) for generic Hamiltonian simulation programs, thereby bridging the gap between impactful quantum applications and physically implementable solutions. Classical simulation of quantum circuits remains a central tool for quantum computing research—including developing and testing quantum algorithms as well as comparing classical computers; therefore, the fifth and sixth papers discuss efficient methods for Schrödinger-style simulations based on joint cutting and cross-platform (CPU and Nvidia GPU) optimization and high-performance backend support.

- **EPOC: A Novel Pulse Generation Framework Incorporating Advanced Synthesis Techniques for Quantum Circuits**
  Jinglei Cheng, University of Pittsburgh, US; Yuchen Zhu, Yidong Zhou, Zhiding Liang, Rensselaer Polytechnic Institute, US; Hang Ren, University of California, Berkeley, US; Zhixin Song, Georgia Institute of Technology, US
- **Assessing Quantum Layout Synthesis Tools via Known Optimal-SWAP Cost Benchmarks**
  Shuohao Ping, Wan-Hsuan Lin, Daniel Bochen Tan, Jason Cong, University of California, Los Angeles, US
- **A Scalable and Robust Compilation Framework for Emitter-Photonic Graph State**
  Xiangyu Ren, Antonio Barbalace, University of Edinburgh, GB; Yuexun Huang, University of Chicago, US; Zhiding Liang, Rensselaer Polytechnic Institute, US
- **Phoenix: Pauli-Based High-Level Optimization Engine for Instruction Execution on NISQ devices**
  Zhaohui Yang, Chenghong Zhu, Yuan Xie, Hong Kong University of Science and Technology, HK; Dawei Ding, Jianxin Chen, Tsinghua University, CN
- **Joint Cutting for Hybrid Schrödinger-Feynman Simulation of Quantum Circuits**
  Laura Herzog, Lukas Burgholzer, Robert Wille, Technical University of Munich, DE; Christian Ufrecht, Daniel Scherer, Fraunhofer IIS/EAS, DE
- **Versatile Cross-Platform Compilation Toolchain for Schrodinger-Style Quantum Circuit Simulation**
  Yuncheng Lu, Shuang Liang, Hongxiang Fan, Ce Guo, Paul Kelly, Wayne Luk, Imperial College London, GB

Session Chair(s): Alberto Marchisio, NYU; Zhiding Liang, Rensselaer Polytechnic Institute

FROM PIXELS TO CHIPS: AI-ENHANCED LAYOUT & MASK DESIGN

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: This session explores how Generative AI is revolutionizing semiconductor design, particularly in the realm of lithography and mask optimization. Discover how large vision models are enabling full-chip mask optimization and how self-supervised deep learning accelerates inverse lithography, pushing the boundaries of resolution and fidelity. We will showcase AI-driven pattern generation techniques for design rule compliance and explore the use of meta-learning to achieve generalizable hotspot detection. Learn how these approaches enable precision-aware yield optimization and ultimately, faster, more efficient chip design. Join us to witness the power of AI in next-generation DFM!

- **LVM-MO: A Large Vision Model Pioneer for Full-Chip Mask Optimization**
  Yiwen Wu, Yuyang Chen, Nan Wang, Tao Wu, Xuming He, Hao Geng, Jingyi Yu, ShanghaiTech University, CN; Shuo Yin, The Chinese University of Hong Kong, HK
- **SSDL-ILT: Efficient ILT Utilizing a Self-Supervised Deep Learning Model**
  Rui Xu, Zhangjiang Laboratory, CN; Junqi Yang, Ming Fang, Zhangjiang Laboratory, CN; Haoxiang Jiang, Shanghai Jiao Tong University, CN
- **PatternPaint: Practical Layout Pattern Generation Using Diffusion-Based Inpainting**
  Guanglei Zhou, Chen-Chia Chang, Jingyu Pan, Yiran Chen, Duke University, US; Bhargav Korrapati, Gaurav Reddy, Dipto Thakurta, Intel Corporation, US; Jiang Hu, Texas A&M University, US

- **Generalizable Lithographic Hotspot Detection Using Asynchronous Meta-Learning with Only One Shot**
  Cong Jiang, Yujia Wang, Dan Feng, Kang Liu, Huazhong University of Science and Technology, CN; Haoyu Yang, Nvidia, US
- **Accuracy Is Not Always We Need: Precision-Aware Bayesian Yield Optimization**
  Jing Kou, Liang Zhang, Haiyan Qin, Wang Kang, Beihang University, CN; Zidong Chen, Wei Xing, The University of Sheffield, GB
- **Curvilinear Optical Proximity Correction via Cardinal Spline**
  Su Zheng, Ziyang Yu, Bei Yu, Martin Wong, The Chinese University of Hong Kong, HK; Xiaoxiao Liang, Yuzhe Ma, The Hong Kong University of Science and Technology, Guangzhou, CN

Session Chair(s): Iris Hui-Rui Jiang, National Taiwan University; Luigi Capodieci, Synopsys, Inc.

LEVERAGING THE MEMORY HIERARCHY FOR EMERGING APPLICATIONS AND HARDWARE

Time: 1:30 PM - 3:00 PM

Topic Area(s): Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: This session discusses innovations in memory hierarchy management for data-intensive applications. It explores the use of In-Memory computing, cache management for emerging neural and graphical processors, the use of disaggregated memory across several hosts, and how to make memory robust. Great progress has been shown toward reducing the performance gap between novel computing architectures and memory.

- **MIRACLE: Multimodal Information Retrieval via a Combined In-Memory Processing and Content Addressable Memory Approach**
  Xuehui Liu, Xueyan Wang, Chen Cheng, Beihang University, CN; Tianyang Yu, Shuo Ran, Bi Wu, Nanjing University of Aeronautics and Astronautics, CN; Xiaotao Jia, Beihang University, CN; Weiqiang Liu, Nanjing University of Aeronautics and Astronautics, CN; Gang Qu, Univ. of Maryland, College Park, US; Weisheng Zhao, Beihang University, CN
- **REMU: Memory-Aware Radiation Emulation via Dual Addressing for In-Orbit Deep Learning System**
  Longnv Xu, Meiqi Wang, Han Qiu, Jun Liu, Yuanjie Li, Hewu Li, Tsinghua University, CN
- **HIVE: A High-Priority Victim Cache for Accelerating GPU Memory Accesses**
  Yuhan Tang, Jianmin Zhang, Sheng Ma, Tiejun Li, Hanqing Li, Luo Shengbai, Jixuan Tang, Lizhou Wu, National University of Defense Technology, CN
- **NVR: Vector Runahead on NPUs for Sparse Memory Access**
  Hui Wang, Jing Wang, Yushu Du, Xiaomeng Han, Dean You, Zhe Jiang, Southeast University, CN; Zhao Zhengpeng, Huazhong University of Science and Technology, CN; Yuan Cheng, Nanjing University, CN; Guo Bing, Wuhan University of Technology, CN; He Xiao, Harbin Institute of Technology, CN; Chenhao Ma, Nanjing Institute of Technology, CN; Jiapeng Guan, Dalian University of Technology, CN; Ran Wei, Lancaster University, GB; Dawei Yang, Houmo, CN
- **Expanding Logical Space Freely: A Memory-Efficient Mapping Table Design for Compressional SSDs**
  Zixuan Huang, Kecheng Huang, Zelin Du, Zili Shao, The Chinese University of Hong Kong, HK; Tianyu Wang, Shenzhen University, CN
- **Sphinx: A High-Performance Hybrid Index for Disaggregated Memory with Succinct Filter Cache**
  Jingxiang Li, Shengan Zheng, Bowen Zhang, Hankun Dong, Linpeng Huang, Shanghai Jiao Tong University, CN

Session Chair(s): Chun-Feng Wu, NYCU; Yi Wang, Shenzhen University

NEW FRONTIERS IN MICROARCHITECTURAL AND PHYSICAL ATTACKS AND DEFENSES

Time: 1:30 PM - 3:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3006, Level 3

Description: Modern computing systems face growing threats from microarchitectural and physical attacks, address these attacks are critical areas of research. This hardware security session showcases novel research on emerging threats and defense mechanisms. The selected papers present state-of-the-art security research on microarchitectural vulnerabilities, including those exploiting timing and speculation, advancements in power side-channel analysis, and security studies on physically unclonable functions (PUFs) and logic locking.

- **RAGNAR: Exploring Volatile-Channel Vulnerabilities on RDMA NIC**
  Yunpeng Xu, Yuchen Fan, Shuwen Deng, Tsinghua University, CN Teng Ma, Renmin University of China, CN;
- **Data Oblivious CPU: Micro-Architectural Side-Channel Leakage-Resilient Processor**
  Behnam Omidi, Khaled N. Khasawneh, George Mason University, US; Ihsen Alouani, Queen's University Belfast, GB
- **"OOPS!": Out-Of-Band Remote Power Side-Channel Attacks on Intel SGX and TDX**
  Nimish Mishra, Kislay Arya, Sarani Bhattacharya, Debdeep Mukhopadhyay, Indian Institute of Technology, Kharagpur, IN; Paritosh Saxena, Intel Corporation, US

- **POLARIS: Explainable Artificial Intelligence for Mitigating Power Side-Channel Leakage**
  Tanzim Mahfuz, Tasneem Suha, Prabuddha Chakraborty, University of Maine, US; Sudipta Paria, Swarup Bhunia, University of Florida, US
- **SCONE: A Logic Locking Technique Utilizing SMT Solver and Circuit Encoding Scheme for Efficient Hardware IP Protection**
  Zhaokun Han, Jeyavijayan Rajendran, Texas A&M University, US; Daniel Xing, Ankur Srivastava, University of Maryland, US; Kostas Amberiadis, NIST, US
- **DeepPUFSCA: Deep Learning for Physical Unclonable Function Attack Based on Side Channel Analysis Support**
  Ngoc Phu Doan, Tuan Dung Pham, Zichi Zhang, Viet Hung Tran, Jack Miskelly, Hans Vandierendonck, Anh Tuan Hoang, Maire O'Neill, Thai Son Mai, Queen's University Belfast, GB

Session Chair(s): Tinoosh Mohsenin, JHU; Sazadur Rahman, University of Central Florida

OPTIMIZING LARGE LANGUAGE MODELS: SPEED, SIZE, AND SMARTS

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session highlights advancements in optimizing large language models (LLMs) for more efficient inference and communication. The papers cover strategies such as pruning, quantization, and adaptive sparse gradient compression, along with methods to reduce communication costs and improve inference speed. These techniques address challenges in long-context processing, multi-modal inference, and chip-level optimizations, all crucial for scaling LLMs in real-world applications.

- **Grasp: Group-Based Prediction of Activation Sparsity for Fast LLM Inference**
  Jiho Shin, University of Seoul, KR; Hoeseok Yang, Santa Clara University, US; Youngmin Yi, Sogang University, KR
- **DuQTTA: Dual Quantized Tensor-Train Adaptation with Decoupling Magnitude-Direction for Efficient Fine-Tuning of LLMs**
  Haoyan Dong, Hai-Bao Chen, Jingjing Chang, Yixin Yang, Ziyang Gao, Zhigang Ji, Shanghai Jiao Tong University, CN; Runsheng Wang, Ru Huang, Peking University, CN
- **PacTrain: Pruning and Adaptive Sparse Gradient Compression for Efficient Collective Communication in Distributed Deep Learning**
  Yisu Wang, Ruilong Wu, Xinjiao Li, Dirk Kutscher, The Hong Kong University of Science and Technology, Guangzhou, CN
- **MILLION: Mastering Long-Context LLM Inference Via Outlier-Immunized KV Product Quantization**
  Zongwu Wang, Peng Xu, Fangxin Liu, Yiwei Hu, Li Jiang, Shanghai Jiao Tong University, CN Qingxiao Sun, CN University of Petroleum, Beijing, CN; Gezi Li, Cheng Li, Xuan Wang, Huawei, CN
- **AASD: Accelerate Inference by Aligning Speculative Decoding in Multimodal Large Language Models**
  Chaoqun Yang, Tsinghua University, CN; Ran Chen, Peking University, CN; Muyang Zhang, Yuzhi Chen, Rongtao Xu, Chinese Academy of Sciences, CN; Weiguang Pang, Kexue Fu, Changwei Wang, Longxiang Gao, Qilu University of Technology, CN
- **ChipAlign: Instruction Alignment in Large Language Models for Chip Design via Geodesic Interpolation**
- Chenhui Deng, Yunsheng Bai, Haoxing Ren, Nvidia, US

Session Chair(s): You Li, Northwestern University; Biresh Joardar, University of Houston

THE ANSWER IS IN-MEMORY!? ... IN THE MEMORY? ... MEMORY? FIND OUT HERE!

Time: 1:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: As data-intensive applications push conventional computing to its limits, in-memory computing emerges as a transformative paradigm to overcome critical memory bottlenecks. This session explores cutting-edge advances in compute-in-memory architectures, showcasing their potential to revolutionize AI acceleration, large-scale similarity search, and Boolean satisfiability solving. We delve into innovative solutions including energy-efficient vector search in NAND flash and DRAM (using UPMEM), adaptive mixed-signal in-memory SAT solvers, and novel CAM- and LUT-based accelerators. The session also highlights state-of-the-art simulation frameworks and stochastic computing techniques that significantly enhance programmability and efficiency.

- **FeKAN: Efficient Kolmogorov-Arnold Networks Accelerator Using FeFET-Based CAM and LUT**
  Xuliang Yu, Yu Qian, Xunzhao Yin, Cheng Zhuo, Liang Zhao, Zhejiang University, CN
- **Energy-Efficient Large-Scale Vector Similarity Search in NAND-Flash via Hybrid Matching**
  Chih-Yu Hu, Chi-Tse Huang, Hao-Wei Chiang, An-Yeu (Andy) Wu, National Taiwan University, TW; Hsiang-Yun Cheng, Academia Sinica, TW; Po-Hao Tseng, Ming-Hsiu Lee, Macronix International Co. Ltd, TW

- **Chameleon-SAT: An Adaptive Boolean Satisfiability Accelerator Using Mixed-Signal In-Memory Computing for Versatile SAT Problems**
  Iris Ying Chou, Hao Kong, Yi Huang, Jianfeng Zhu, Wenping Zhu, Shaojun Wei, Aoyang Zhang, Leibo Liu, Tsinghua University, CN
- **A Full-System, Programmable, and Extensible In-Memory Computing Simulation Framework for Deep Learning**
  Kaining Zhou, Jian Huang, Nam Sung Kim, Naresh Shanbhag, University of Illinois at Urbana-Champaign, US
- **All-in-Memory Stochastic Computing Using ReRAM**
  Joao Paulo De Lima, Jeronimo Castrillon, Asif Ali Khan, Technische Universität Dresden, DE; Mehran Shoushtari Moghadam, M. Hassan Najafi, Case Western Reserve University, US; Sercan Aygun, University of Louisiana at Lafayette, US
- **UPVSS: Jointly Managing Vector Similarity Search with Near-Memory Processing Systems**
  Chun-Chien Liu, Chun-Feng Wu, National Yang Ming Chiao Tung University, TW; Yunho Jin, Harvard University, US

Session Chair(s): Hussam Amrouch, Technische Universitat Munchen; Giacomo Pedretti, Hewlett Packard Enterprise

TRANSFORMERS: RISE OF THE OPTIMIZED LARGE LANGUAGE MODELS

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: This session is about transformers and large language model optimizations. As LLMs are essentially made of transformers due to their superior effectiveness to understand context and relationships within sequences by using self-attention mechanism, their hardware optimizations are quite important. We have a best paper award candidate presentation for DRAFT, which is about a clever hardware technique that approximates the backpropagation hardware for great energy efficiency improvement. Our other papers cover hardware/algorithm co-design, retrieval-in-memory techniques, attention, long-context generation, and an overview of the pareto-frontier for low-precision data formats.

- **SSFT: Algorithm and Hardware Co-Design for Structured Sparse Fine-Tuning of Large Language Models**
  Miao Yu, Trevor E. Carlson, National University of Singapore, SG
- **DRAFT: Decoupling Backpropagation from Pre-trained Backbone for Efficient Transformer Fine-Tuning on Edge**
  Zhirui Huang, Shiwei Liu, Haozhe Zhu, Qi Liu, Chixiao Chen, Fudan University, CN
- **Move Less, Retrieve Fast: A Retrieval-in-Memory Architecture for Language Models**
  Jiaxian Chen, Yuxuan Qi, Jianan Yuan, Kaoyi Sun, Tianyu Wang, Chenlin Ma, Yi Wang, Shenzhen University, CN
- **KVO-LLM: Boosting Long-Context Generation Throughput for Batched LLM Inference**
  Zhenyu Li, Dongxu Lyu, Gang Wang, Yuzhou Chen, CN; Liyan Chen, Wenjie Li, Jianfei Jiang, Yanan Sun, Guanghui He, Shanghai Jiao Tong University, CN
- **An Energy-Efficient High-Utilization Hardware Architecture for Attention Mechanism in Transformer using Balanced Systolic Array and Multi-Row Interleaved Operation Ordering**
  Haiyang Zhou, Hongyang Hu, Jinshan Yue, Hanghang Gao, Yuanlu Xie, Xiaoxin Xu, Chunmeng Dou, Institute of Microelectronics of Chinese Academy of Sciences, CN; Ming Liu, Fudan University, CN
- **Finding the Pareto Frontier of Low-Precision Data Formats and MAC Architecture for LLM Inference**
  Brian Crafton, Xiaochen Peng, Xiaoyu Sun, Ashwin Lele, Bo Zhang, Win-San Khwa, Kerem Akarvardar, TSMC, US

Session Chair(s): Abdelrahman Hosny, Apple; Marina Neseem, Nvidia

PERFORMANCE VS. SUSTAINABILITY: THE CHALLENGE OF ENERGY-EFFICIENT COMPUTING

Time: 1:30 PM - 3:00 PM

Topic Area(s): Systems

Session Type: Panel

Room: 2012, Level 3

Description: In today's state-of-the-art technology, High-Performance computing (HPC) is paramount to solve complex scientific and business problems. Some of the key challenges of HPC is the power consumption, scalability limitations, and the rapid pace of hardware innovation making it difficult to keep systems up to date. All these factors lead to a potentially unsustainable situation.

With that, Sustainable and Energy-Efficient computing paradigm has become extremely critical. By using technological advancement, we need to maximize energy efficiency, reduce resource consumption, and promoting recycling of electronic waste throughout the product lifecycle.

In this panel, we will discuss various ways to achieve Sustainability and Energy-Efficient Computing. While all the panelists believe that Energy-Efficiency and Sustainability needs to be achieved, there is a wide variety of opinions and disagreements about the way to achieve that. Significant amount of research needs to be performed in various angles mentioned by the panelists.

Organizer(s): Sabya Das, Synopsys, US

Moderator: Rob Aitken, U.S. Department of Commerce, US

Speakers: Ankireddy Nalamalpu, VP, MediaTek, US; Peter Beerel, University of Southern California, US; Jeanne Trinko-Mechler, Marvell Technology, US; Jae-sun Seo, Cornell University, US; Ilya Ganusov, Altera, US; Rick Crotty, Lattice Semiconductor, US

ADVANCING QUANTUM COMPUTING FOR TOMORROW

Time: 1:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: As quantum computing advances toward practical applications, a deeper exploration of Noisy Intermediate-Scale Quantum (NISQ) technologies is essential. This session, "Advancing Quantum Computing for Tomorrow," brings together experts from industry, national laboratories, and academia to discuss key challenges and opportunities in the evolving quantum ecosystem. Topics include quantum system co-design, hybrid quantum-classical integration, quantum error correction, and scientific applications, with a focus on optimizing NISQ performance through scalable hardware, software architectures, and error mitigation strategies. By bridging advancements in hardware and software, this session highlights the transformative potential of quantum computing across chemistry, materials science, artificial intelligence, and beyond, providing attendees with a comprehensive perspective on its future impact in science, technology, and industry.

- **Co-design of Quantum Processors for NISQ Applications**
- **John Gamble, IONQ, US**
- **Accelerated Quantum Supercomputing**
- **Jin-Sung Kim, Nvidia, US**
- **Quantum Computers and Their Role in Enabling Scientific Discovery**
- **Costin Iancu, LBNL, US**

Session Chair(s): Fan Chen, Indiana University, US; Samah Saeed, City University of New York, US

STATIC SIGN-OFF METHODOLOGIES: LIBERATING FUNCTIONAL VERIFICATION FROM BOOLEAN SHACKLES

Time: 1:45 PM - 2:15 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Engineering teams are increasingly prioritizing early functional verification, achieving targeted verification and sign-off across more domains during RTL design—well before simulation. This early sign-off approach dramatically reduces downstream engineering changes and iterations.

Successfully deploying sign-off during RTL design requires both tool speed and the scalability to handle IPs and SoCs, along with complete coverage that detects all targeted errors.

Because static sign-off leverages abstract checking methods rather than the Boolean analysis used by simulation and formal verification, it delivers 10–100X faster runtimes, multi-billion-gate capacity, and a more efficient setup process. Additionally, its support for user-defined rules enables in-depth analysis for emerging applications where design requirements continue to evolve.

Multiple experts will share production-proven methodology advances and best practices across key static sign-off applications, including: 1) RTL linting, 2) clock domain crossing, 3) reset domain crossing, 4) design-for-testability, 5) connectivity and glitch detection, and 6) hardware security sign-off.

Attendees will gain a deeper understanding of static sign-off methodologies, along with practical insights tailored to specific applications.

Speakers: Prakash Narain, Kanad Chakraborty, Sanjay Thatte, Lisa Piper, Vikas Sachdeva, Real Intent, US

GENERATIVE AI IN DESIGN & VERIFICATION: ARE WE HALLUCINATING OR INNOVATING?

Time: 2:00 PM - 2:45 PM

Topic Area(s): AI

Session Type: DAC Pavilion Panel

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The rapid rise of generative AI holds the promise of transforming semiconductor design and verification flows with unprecedented capabilities in automation, intelligent synthesis, and error detection. Enthusiasts envision a future where AI accelerates innovation cycles, reduces costs, and addresses the growing complexity of chip design with ease. However, skeptics question whether these expectations are grounded in reality, pointing to challenges like the "black box" nature of AI models, lack of explainability, and potential over-reliance on technology that may not yet be mature.

This panel brings together leading voices representing both ends of the spectrum to tackle a critical question: Are we innovating responsibly with generative AI, or are we risking costly illusions? Champions of generative AI will argue that the technology is already enabling significant advancements, from automating repetitive tasks to uncovering design optimizations that were previously unfeasible. On the other side, cautious experts will highlight the risks of blindly adopting AI-driven solutions, including trust deficits, bias in decision-making, and the potential to exacerbate the talent shortage by creating new skill demands that the current workforce may struggle to meet.

The panelists will debate key points of contention, such as:

Accuracy vs. Reliability: Can generative AI provide the level of precision required for mission-critical designs, or do its inherent limitations in explainability make it a liability in high-stakes environments?

Automation vs. Creativity: Does AI enable engineers to focus on higher-level problem solving, or does it risk stifling creativity by promoting over-automation and reliance on pre-trained models?

Short-term Gains vs. Long-term Impacts: Are current generative AI applications genuinely reducing time-to-market, or are they introducing new complexities and risks that could offset these benefits in the long run?

Workforce Transformation: Will generative AI alleviate the talent shortage by streamlining workflows, or will it deepen the skills gap by demanding expertise in both AI and traditional design methodologies?

Trust and Governance: How do we ensure that AI-generated solutions are transparent, verifiable, and aligned with industry standards?

Join us for this dynamic and thought-provoking discussion as our panelists confront these challenges head-on and seek to separate innovation from illusion. Together, we'll explore the tangible opportunities, the realistic timelines for adoption, and the strategies needed to ensure that generative AI drives sustainable progress in semiconductor design and verification. Whether you're an optimist, a skeptic, or somewhere in between, this panel promises insights to inform your perspective on the future of design automation.

Moderator: Brian Bailey, Semiconductor Engineering, US

Panelists: Alon Shtepel, Micron, US; Abhi Kolpekwar, Siemens, US

MASTERING MODERN DATA MANAGEMENT: INSIGHTS AND CASE STUDIES

Time: 2:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: This session dives into advanced data management strategies using Keysight's Design Data Management (SOS), backed by real-world case studies. We'll showcase how Keysight SOS delivers unmatched flexibility in managing any kind of design or engineering data—structured or unstructured—across today's most demanding, multi-site environments.

Learn how Keysight SOS unifies fragmented toolchains by integrating with third-party SCM systems like Git, enabling seamless hybrid workflows while maintaining a single source of truth. We'll demonstrate how to harness Keysight SOS triggers to automate workflows, enforce governance, and accelerate development cycles. The presentation also highlights performance-driven features such as links-to-cache, sparse populate, and reference-based reuse—powerful tools that dramatically reduce storage overhead, boost speed, and scale collaboration without compromise. Whether you're managing IP, source code, test data, or complex hardware designs, this session will show how Keysight SOS transforms design data management into a streamlined, automated, and scalable operation—built for the realities of modern engineering.

Speaker: Pedro Pires, Keysight Technologies, US

COOLEY'S DAC TROUBLEMAKER PANEL

Time: 3:00 PM - 4:00 PM

Topic Area(s): EDA

Session Type: DAC Pavilion Panel

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old-style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

Moderator: John Cooley, Deepchip, US

Panelists: Mike Ellow, Siemens; Ravi Subramanian, Synopsys; Paul Cunningham, Cadence Design Systems, Inc.; Dean Drako, IC Manage; Prakash Narain, Real Intent; Sam Appleton, Ausdia

BUILDING TRUST IN GENAI FOR SEMICONDUCTOR DESIGN: ADDRESSING DATA PROVENANCE, QUALITY, AND TRACEABILITY CHALLENGES

Time: 3:30 PM - 4:00 PM

Topic Area(s): AI, Design

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The semiconductor industry is on the cusp of an AI revolution, yet significant barriers persist, particularly around data provenance and liability. While Generative AI (GenAI) technologies have transformed software development, their adoption in semiconductor design remains hindered by the industry's unique challenges—such as highly protected intellectual property (IP) and the extraordinary costs associated with errors. Unlike the software domain, where open-source practices are common, the hardware space demands a more secure and traceable approach.

This presentation will explore the emerging role of GenAI in semiconductor and embedded systems design, focusing on the critical issues of data versioning, provenance, and traceability in training internal AI models. These factors are essential to ensure model reproducibility, reliability, and accountability, as well as to mitigate risk and foster trust in AI adoption. We will explore concerns around "data contamination" when using external or purchased IP as well as liability concerns over whether such data can lawfully and ethically be used to train AI.

Additionally, we will introduce IP Lifecycle Management (IPLM) as a robust framework for managing and tracking the IPs used in AI training. By leveraging an IPLM platform, organizations can establish a secure, compliant, and controlled approach to training AI models, paving the way for innovative applications in semiconductor design.

Speaker: Vishal Moondhra, Perforce Software, US

BACK-END AND SYSTEM CONSIDERATIONS FOR CHIPLETS

Time: 3:30 PM - 5:00 PM

Topic Area(s): Systems and Software

Session Type: Engineering Track

Room: 2008, Level 2

Description: Join us for a comprehensive session that explores the latest advancements in chiplet integration and 3DIC design, focusing on security, optimization, and thermal management, offering valuable insights into cutting-edge methodologies that enhance the reliability, efficiency, and performance of modern SoC and 3DIC systems. We start with a deep dive into secure chiplet integration within System-in-Package (SiP) architectures, detailing methods for secure authentication, remote attestation, and data protection through cryptographic techniques. Next, discover how to leverage machine learning to optimize heterogeneous 3DIC designs, significantly enhancing power, performance, and area (PPA) metrics through automated design space exploration. Explore SuperCoverage, an AI-guided approach that exponentially increases workload coverage for power and thermal analysis, ensuring accurate hot-spot temperature measurements crucial for dynamic power and thermal control. Learn about the complexities of Electrostatic Discharge (ESD) in multi-die systems, and learn how novel simulation tools can identify potential ESD vulnerabilities in 3DIC designs. This session will also coveradvanced thermal simulation techniques for 3DIC packages with co-packaged optics, addressing thermal cross-talk and ensuring thermal integrity. Lastly, discover high-performance extraction methods for 2.5D/3D-IC packages, utilizing hybrid computational electromagnetic frameworks and machine learning to streamline the design process.

- **Securing Chiplet Integration: A System-in-Package Security Architecture**
  Sylvain Guilley, Secure-IC, FR; Junie Um, Cadence Design Systems, Inc., US
- **Heterogenous 3DIC Partitioning with Cerebrus Machine Learning for PPA Optimization**
  Yi-Wei Chen, Chung-Ching Peng, Yi-Shan Li, Kuan-Ting Kuo, Vivek Rajan, Intel Corporation, US; Narendra Akilla, Stephen Morais, Xukang Wu, Naresh Mummidivarapu, Kumar Subramani, Cadence Design Systems, Inc., US
- **SuperCoverage: AI-Guided Full Coverage of Thermal and Power Analysis for SoC Design**
  Xia Zhu, Jianfang Zhu, Mark Gallina, Julien Sebot, Intel Corporation, US
- **Analysis of Electrostatic Discharge (ESD) for 3DIC Systems**
  Anila Azam, Intel Corporation, US

- **Accurate Thermal Simulation of 3DIC Package with Co-Packaged Optics**
  Ahsan Alam, Qinglian Li, Lucy Yin, Lang Lin, Wenbo Xia, Ansys, US
- **High Performance Extraction of 2.5D/3D-IC Package**
  Xiaoyan Xiong, Yingxin Sun, Jiyue Zhu, Gang Kang, Jian Liu, Cadence Design Systems, Inc., US

Session Chair(s): Frank Schirrmeister, Synopsys, US

CUSTOM IP BLOCKS – THE LEGO BLOCKS OF DIGITAL DESIGN

Time: 3:30 PM - 5:00 PM

Topic Area(s): IP

Session Type: Engineering Track

Room: 2010, Level 2

Description: Hardened IP blocks, from the humble inverter to the multimillion transistor SRAM macro, are the basis without which digital design cannot exist. Creating, extracting and characterizing them is therefore a crucial step in their generation flow. This session describes techniques for the design and view generation of hard IP that help achieve the optimal PPA results.

- **Scenario-Based Mixed Signal Layout Generator Using Generation APIs for Memory**
  Jeongyoon Lee, Kyeongrok Jo, Seungkwang Hong, Sichan Kim, Seunghwan Lee, Youngwook Kim, Jungyun Choi, Samsung, KR
- **Logic and SRAM Library Generation and Analysis for Digital Design Enablement**
  Sravanth Mucharla, Shruti Rakheja, Google, IN; Ray Shane Toma, Siemens, CA
- **Novel IC Layout Parasitics Analysis Techniques to Enhance Custom Macro/IP and Standard Cell Library Development Flow**
  Ravi J N, Kopal Kulshreshtha, Maxim Ershov, Ansys, SE; Pramod Gayakwad, Santhosh Kamatam, NXP Semiconductor, IN
- **An Engineering Approach to High Performance Scannable Flip Flops Embedding Functional Logics**
  Min-su Kim, Yong Geol Kim, Daeseong Lee, Hyoungwook Lee, Samsung, KR
- **Robust Hard Macro Timing Validation: Early Detection of Issues and Automated Feedback for Integration**
  Vaibhav Garg, Mohita Batra, Arjun Saha, Rishabh Srivastava, Synopsys, IN
- **Robust Verification for Complex Liberty IP**
  Ray Valencia, Siemens, CA; Ajay Kumar, Siemens, GB; Santhosh Kamatam, Khushboo Rathore, Pramod Gayakwad, NXP, IN

Session Chair(s): Nanditha Rao, IBM, IN

SLM IS THE NEW DFT – ARE YOU READY?

Time: 3:30 PM - 5:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2010, Level 2

Description: It's Monday morning, and you get pulled into an ad-hoc meeting to discuss your latest SoC's performance and power targets. The chip is missing performance targets by 15%, and now your team needs to raise the power budget to meet the spec. The entire process devolves into a flurry of finger-pointing without concrete evidence of what went wrong. When it comes to your $200M SoC project, is it better to guess or know what went wrong?

Most modern SoCs mitigate the guesswork by leveraging DFT (Design for Test) techniques, like adding more memory BIST or improving functional coverage. However, these tests were meant for verifying connectivity and basic functionality. What happens when you need the next level of observability and analytics to improve power, performance, yield, and reliability? These next-level analytics are driving the adoption of silicon lifecycle management (SLM) platforms.

For those unfamiliar, SLM platforms combine a variety of specialized on-die sensors with an analytics engine to improve power margins, manufacturing yield, silicon longevity, failure analysis, and enable predictive maintenance. The targeted analytics enable design optimizations at each stage of the design lifecycle, including pre-silicon through in-field operations.

As SoCs grow in size, complexity, and cost, expanding visibility is important. SLM is not yet broadly adopted in the industry, but just like DFT went from a concept to a norm SLM is expected to follow the same path.

Our discussion will briefly explore the current state of silicon testing and its evolution from bench characterization and ATE to in-field testing. It will also delve into different silicon lifecycle solutions and how they fit in each design phase. Together, we will answer some of the following questions from an IP, analytics platform, and testing perspective:

- How is testing done today?
- What are the limitations, and how can they be overcome?
- If the new test capabilities include the ability to test in the field, what benefits does that bring/how can that capability be leveraged?
- What is required to enable this capability, and how does it affect system architecture?
- How does this impact test at the ATE, chiplet, SLT, and in-field stages?
- What is the adoption path for this technology?

Organizer(s): Aakash Jani, Movellus

Moderator: Ann Mutschler, Semiconductor Engineering, US

Speakers: Geir Eidi, Siemens, US; Steve Pateras, Synopsys, US; Ken Butter, Advantest, US; Vikram Karvat, Movellus, US

FROM SIMULATION TO THREATS, A DEEP-DIVE INTO CPS AND IOT DESIGN

Time: 3:30 PM - 5:30 PM

Topic Area(s): Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: The design of Cyber-Physical Systems (CPS) and Internet of Things (IoT) devices is a well-known challenging process. This session explores key stages of the design flow, including system simulation, optimization, and management. A variety of target platforms, ranging from RISC-V-like architectures to FPGA-based accelerators, will be covered. Additionally, advanced design space exploration and task-scheduling algorithms will be presented to address fundamental and compelling aspects of CPS and IoT scenarios, such as energy awareness and robustness against attacks.

- **Fast End-to-End Simulation and Exploration of Many-Core Baseband Transceivers for Software-Defined Radio-Access Networks**
  Marco Bertuletti, Yichao Zhang, Samuel Riedel, ETH Zürich, CH; Mahdi Abdollahpour, Alessandro Vanelli-Coralli, Luca Benini, Universita' di Bologna, IT
- **Intermittent Systems at Small Scale: Execution Model and Design Guidelines**
  Youngbin Kim, Yoojin Lim, ETRI, KR
- **MEEK: Re-Thinking Heterogeneous Parallel Error Detection Architecture for Real-World OoO Superscalar Processors**
  Zhe Jiang, Dean You, Southeast University, CN; Minli Liao, Timothy Jones, University of Cambridge, GB; Sam Ainsworth, University of Edinburgh, GB
- **VersaSlot: Efficient Fine-Grained FPGA Sharing with Big.Little Slots and Live Migration in FPGA Cluster**
  Jianfeng Gu, Hao Wang, Xiaorang Guo, Martin Schulz, Michael Gerndt, Technical University of Munich, DE
- **Power-Constrained Printed Neuromorphic Hardware Training**
  Tara Gheshlaghi, Haibin Zhao, Priyanjana Pal, Michael Beigl, Mehdi Tahoori, Karlsruhe Institute of Technology, DE; Michael Hefenbrock, RevoAI GmbH, DE
- **Age-of-Information Minimization for Data Aggregation in Energy-Harvesting IoTs**
  Bingkun Yao, Nan Guan, City University of Hong Kong, HK; Mun Choon Chan, National University of Singapore, SG; Hong Gao, Zhejiang Normal University, CN; Zhe Jiang, Southeast University, CN
- **Uncertainty-Aware Energy Management for Wearable IoT Devices with Conformal Prediction**
  Dina Hussein, Chibuike Ugwu, Ganapati Bhat, Jana Doppa, Washington State University, US
- **Query-Based Black-Box Stealthy Sensor Attacks on Cyber-Physical Systems**
  Shixiong Jiang, Weizhe Xu, Mengyu Liu, Fanxin Kong, University of Notre Dame, US

Session Chair(s): Stefano Di Carlo, Politecnico di Torino; Hokeun Kim, Arizona State University

MODELS AND HARDWARE FOR MACHINE LEARNING AND BEYOND

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3003, Level 3

Description: In this session, we will present eight works on hardware and algorithm design for emerging computing models. These span a wide range of areas, including AI, machine learning, neuromorphic computing, bioinformatics, approximate computing, and biochips. The selected works feature novel algorithms and hardware architectures for both general AI and machine learning applications, as well as specialized AI models such as vector symbolic AI. Together, they showcase a diverse array of computing techniques, highlighting the challenges and state-of-the-art solutions within these evolving paradigms.

- **Pipirima: Predicting Patterns in Sparsity to Accelerate Matrix Algebra**
  Ubaid Bakhtiar, Donghyeon Joo, Bahar Asgari, University of Maryland, College Park, US
- **FactorHD: A Hyperdimensional Computing Model for Multi-Object Multi-Class Representation and Factorization**
  Yifei Zhou, Xuchu Huang, Chenyu Ni, Min Zhou, Xunzhao Yin, Cheng Zhuo, Zhejiang University, CN; Zheyu Yan, University of Notre Dame, US
- **Holistic Design Towards Resource-Stringent Binary Vector Symbolic Architecture**
  Shijin Duan, Nuntipat Narkthong, Xiaolin Xu, Northeastern University, US; Yukui Luo, Binghamton University, US; Shaolei Ren, University of California, Riverside, US
- **SDISC: A Spike-Driven Human-Machine Interface with In-Situ Computing for Real-Time Low-Power Interaction**
  Fangduo Zhu, Jingyi Chen, Jingsong Zhang, Xumeng Zhang, Siyuan Ouyang, Chenyang Li, Hao Jiang, Qi Liu, Fudan University, CN; Xiaonan Yang, Zhengzhou University, CN
- **ANGraph: A GNN-Based Performance Prediction Framework for Asynchronous Neuromorphic Hardware**
  Yuan Hua, Jian Zhang, Jilin Zhang, Xiang Zhang, Hong Chen, Tsinghua University, CN

- **PairGraph: An Efficient Search-Space-Aware Accelerator for High-Performance Concurrent Pairwise Queries**
  Yutao Fu, Zhongtian Long, Yu Zhang, Zirui He, Jin Zhao, Qiyuan Niu, Zixiao Wang, Hai Jin, Huazhong University of Science and Technology, CN
- **PreDAC: An Efficient Framework of Pre-Refining Enhanced Design Space Exploration for Approximate Computing**
  Ziying Cui, Ke Chen, Bi Wu, Yu Gong, Chenggang Yan, Weiqiang Liu, Nanjing University of Aeronautics and Astronautics, CN
- **AutoRE: Bayesian-Optimization-Based Automatic Reliability Enhancement Tool for Flow-Based Microfluidic Biochips**
  Siyuan Liang, Tsung-Yi Ho, The Chinese University of Hong Kong, HK; Yushen Zhang, Mengchu Li, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University of Munich, DE

Session Chair(s): Jun Shiomi, The University of Osaka; Cheng Wang, Iowa State University

PUSHING QUANTUM COMPUTING REALITY FROM ROUTING TO ERROR CORRECTIONS AND QML

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3004, Level 3

Description: This session explores new ideas in quantum computing, focusing on qubit routing, qubit readout, reducing errors, error correction, checking the equivalence of quantum circuits, and using quantum machine learning. The first paper aims to solve the qubit routing problem through a novel heuristic algorithm. Quantum readout error is the most significant source of error; therefore, the second, third, and fourth papers present qubit readout architecture leveraging lightweight neural networks, scalable high-fidelity three-level readout, and a software-hardware co-design approach that mitigates readout errors with an embedded accelerator. The fifth paper presents a fast-Ising model-based approach for efficient quantum error correction. The sixth paper discusses a transformative framework for quantum circuit equivalence checking using ZX calculus-based graph abstractions. The seventh and eighth papers focus on quantum machine learning (QML) through amplitude embedding and a framework for efficient and high-accuracy training and inference on heterogeneous quantum processing units.

- **DDRoute: a Novel Depth-Driven Approach to the Qubit Routing Problem**
  Alessandro Annechini, Marco Venere, Donatella Sciuto, Marco Santambrogio, Politecnico di Milano, IT
- **KLiNQ: Knowledge Distillation-Assisted Lightweight Neural Network for Qubit Readout on FPGA**
  Xiaorang Guo, Tigran Bunarjyan, Dai Liu, Martin Schulz, Technical University of Munich, DE; Benjamin Lienhard, Princeton University, US
- **Efficient and Scalable Architectures for Multi-level Superconducting Qubit Readout**
  Chaithanya Mude, Satvik Maurya, Swamit Tannu, University of Wisconsin, Madison, US; Benjamin Lienhard, Princeton University, US
- **DyREM: Dynamically Mitigating Quantum Readout Error with Embedded Accelerator**
  Kaiwen Zhou, Liqiang Lu, Hanyu Zhang, Debin Xiang, Chenning Tao, Xinkui Zhao, Jianwei Yin, Zhejiang University, CN; Size Zheng, Bytedance Inc., CN
- **Weighted Range-Constrained Ising-Model Decoder for Quantum Error Correction**
  Xinyi Guo, Hiromitsu Awano, Takashi Sato, Kyoto University, JP
- **ZXNet: ZX Calculus-Driven Graph Neural Network Framework for Quantum Circuit Equivalence Checking**
  Navnil Choudhury, Ameya Bhave, Kanad Basu, The University of Texas at Dallas, US
- **EnQode: Fast Amplitude Embedding for Quantum Machine Learning using Classical Data**
  Jason Han, Nicholas DiBrita, Hengrui Luo, Rice University, US; Tirthak Patel, Rice University, US; Younghyun Cho, Santa Clara University, US
- **ArbiterQ: Improving QNN Convergency and Accuracy by Applying Personalized Model on Heterogeneous Quantum Devices**
  Tianyao Chu, Siwei Tan, Liqiang Lu, Congliang Lang, Yifan Guo, Jianwei Yin, Zhejiang University, CN; Jingwen Leng, Fangxin Liu, Shanghai Jiao Tong University, CN

Session Chair(s): Jinglei Cheng, University of Pittsburgh; Himanshu Thapliyal, University of Tennessee

READY, SET, SCALE! AI'S JOURNEY FROM EDGE TO CLOUD OPTIMIZATION

Time: 3:30 PM - 5:30 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: As AI models grow in complexity, the need for optimized architectures and efficient inference mechanisms becomes more pressing. This session explores cutting-edge advancements in the optimization of machine learning models, with a focus on efficiency, scaling, and hardware optimization. The first set of presentations delves into innovative approaches for enhancing the efficiency of edge ML models. The middle presentations shift the spotlight to large-scale models, addressing key challenges in dynamic graph processing, scaling laws for GNNs. Finally, the session concludes with a look at GPU-side optimizations, showcasing techniques for efficient scheduling to meet the demanding requirements of large model serving. This diverse range of topics provides a comprehensive view of the future of ML model optimization from edge devices to high-performance computing systems.

- **Can Short Hypervectors Drive Feature-Rich GNNs? Strengthening the Graph Representation of Hyperdimensional Computing for Memory-Efficient GNNs**
  Jihe Wang, Yuxi Han, Danghui Wang, Northwestern Polytechnical University, CN
- **InfScaler: Enabling Efficient ML Inference Serving on Multi-Accelerator Edge Devices via Asymmetric Auto-Scaling**
  Borui Li, Tiange Xia, Shuai Wang, Shuai Wang, Southeast University, CN
- **DM-Tune: Quantizing Diffusion Models with Mixture-of-Gaussian Guided Noise Tuning**
  Pouya Haghi, Ali Falahati, Zahra Azad, Chunshu Wu, Ruibing Song, Chuan Liu, Tong Geng, University of Rochester, US Ang Li, Pacific Northwest National Laboratory, US
- **Towards In-Situ Neuromorphic Computing Architecture for Event Stream Super-Resolution**
  Yihe Yu, Bo Li, Kexin Huang, Wei Liu, Jinghai Wang, Yue Liu, Zhiyi Yu, Shanlin Xiao, Sun Yat-sen University, CN
- **LearnGraph: A Learning-Based Architecture for Dynamic Graph Processing**
  Lingling Zhang, Yijian Wu, Ziyu Zhou, Tiancheng Lu, Capital Normal University, CN; Hong Jiang, The University of Texas at Arlington, US
- **Neural Scaling Laws for Graph Neural Networks in Atomistic Materials Modeling**
  Chaojian Li, Zhifan Ye, Cheng Wan, Georgia Institute of Technology, US; Massimiliano Lupo Pasini, Jong Youl Choi, Prasanna Balaprakash, Oak Ridge National Laboratory, US
- **VISTA: Optimizing GPU Scheduling Through Versatile Locality-Aware Data Sharing**
  Hajar Falahati, Negin Mahani, Adrian Cristal, Osman Unsal, Barcelona Supercomputing Center, ES
- **Tropical: Enhancing SLO Attainment in Disaggregated LLM Serving via SLO-Aware Multiplexing**
  Jinming Ma, Jiangfei Duan, Haojie Duanmu, Xingcheng Zhang, Dahua Lin, Shanghai Artificial Intelligence Laboratory, CN; Jiefei Chen, Fudan University, CN; Xiuhong Li, Chao Yang, Peking University, CN

Session Chair(s): Jinjun Xiong, University at Buffalo; Yoichi Tomioka, University of Aizu, JP

SHAPING TOMORROW: CO-DESIGNING EMERGING TECHNOLOGIES FOR COMPUTING AND BEYOND

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3001, Level 3

Description: The rapid evolution of AI and computing demands innovative co-design approaches that integrate hardware, algorithms, and systems. This session explores cutting-edge research at the intersection of emerging technologies and co-design methodologies. Topics include drift-tolerant neural networks, Compute Express Link (CXL) optimization, ferroelectric and SOT-MRAM compute-in-memory architectures, monolithic 3D integration and in-sensor computing for biomedical diagnostics. By addressing challenges such as energy efficiency, scalability, and performance, these works showcase how co-design can unlock the full potential of advanced technologies for AI and other domains, paving the way for next-generation computing systems.

- **DBC: Drift-Aware Binary Code for Drift-Tolerant Deep Neural Networks**
  Insu Choi, Jaeyong Chung, Joon-Sung Yang, Yonsei University, KR
- **CXL-Interplay: Unraveling and Characterizing CXL Interference in Modern Computer Systems**
  Shunyu Mao, Jiajun Luo, Yixin Li, Shuwen Deng, Tsinghua University, CN; Jiapeng Zhou, Chinese Academy of Sciences, CN; Weidong Zhang, Zheng Liu, Alibaba Group, CN; Teng Ma, Renmin University of China, CN
- **VQT-CiM: Accelerating Vector Quantization Enhanced Transfomer with Ferroelectric Compute-in-Memory**
  Xuchu Huang, Haonan Du, Min Zhou, Cheng Zhuo, Xunzhao Yin, Zhejiang University, CN; Zheyu Yan, University of Notre Dame, US

- **Enhancing Parallelism and Energy-Efficiency in SOT-MRAM based CIM Architecture for On-Chip Learning**
  Anubha Sehgal, Alok Shukla, Sandeep Soni, Sourajeet Roy, Indian Institute of Technology Roorkee, IN; Sumit Diware, Rajendra Bishnoi, Delft University of Technology, NL; Seema Dhull, GlobalFoundries, IN; Sonal Shreya, Aarhus University, DK
- **Device-Algorithm Co-Design of Ferroelectric Compute-in-Memory In-Situ Annealer for Combinatorial Optimization Problems**
  Yu Qian, Xianmin Huang, Ranran Wang, Zeyu Yang, Min Zhou, Cheng Zhuo, Xunzhao Yin, Zhejiang University, CN; Thomas Kämpfe, Fraunhofer IPMS, DE; Kai Ni, University of Notre Dame, US
- **DANN: Diffractive Acoustic Neural Network for In-Sensor Computing System Target at Multi-Biomarker Diagnosis**
  Lewei He, Ning Lin, Binbin Cui, Xinran Zhang, Shiming Zhang, University of Hong Kong, HK; Zhongrui Wang, Southern University of Science and Technology, CN
- **333-eDRAM - 3T Embedded DRAM Leveraging Monolithic 3D Integration of 3 Transistor Types: IGZO, Carbon Nanotube and Silicon FETs**
  David Kong, Shvetank Prakash, Georgios Kyriazidis, Yasmine Omri, Vijay Janapa Reddi, Gage Hills, Harvard University, US; Jedrzej Kufel, David Verity, Emre Ozer, Pragmatic Semiconductor, GB
- **Monolithic 3D FPGA Design and Synthesis with Back-End-of-Line Configuration Memories**
  Faaiq Waqar, Georgia Institute of Technology, US; Jiahao Zhang, Zifan He, Jason Cong, University California, Los Angeles, US; Anni Lu, Shimeng Yu, Georgia Institute of Technology, US

Session Chair(s): Doo Seok, Hanyang University

UNLEASHING THE POWER OF ACCELERATORS: ASICS, FPGAS, AND PIMS

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: This session explores innovative accelerator designs for AI and other applications, leveraging diverse technologies from ASICs and hardware-software co-design to FPGAs and Processing-in-Memory (PIM). The session begins with a cache-aware, multi-tenant DNN accelerator for NPUs. The next paper presents a FPGA-based configurable CAM architecture with multi-query support. Moving to PIM-based acceleration, the next paper explores a co-simulation environment for design space exploration of PIM architectures and Network-on-Chip (NoC) configurations, followed by a presentation on a novel PIM-based LLM accelerator. Next, a memory-efficient Fully Homomorphic Encryption (FHE) processing unit is presented. Finally, the session concludes with three presentations on specialized accelerators targeting vision and brain-computer interface applications.

- **CaMDN: Enhancing Cache Efficiency for Multi-Tenant DNNs on Integrated NPUs**
  Tianhao Cai, Liang Wang, Limin Xiao, Meng Han, Zeyu Wang, Xiaojian Liao, Beihang University, CN; Lin Sun, Jiangsu Shuguang Optoelectric Co., Ltd., CN
- **Configurable DSP-Based CAM Architecture for Data-Intensive Applications on FPGAs**
  Yao Chen, Feng Yu, Weng-Fai Wong, Bingsheng He, National University of Singapore, SG; Di Wu, University of Science and Technology of China, CN
- **HPIM-NoC: A Priori-Knowledge-Based Optimization Framework for Heterogeneous PIM-Based NoCs**
  Shuai Yuan, Angxin Cai, Guoxing Wang, Jianfei Jiang, Guanghui He, Yanan Sun, Shanghai Jiao Tong University, CN; Qiushi Lin, Yu Wang, Zhenhua Zhu, Tsinghua University, CN
- **McPAL: Scaling Unstructured Sparse Inference with Multi-Chiplet HBM-PIM Architecture for LLMs**
  Shiwei Liu, Zhirui Huang, Qi Liu, Chixiao Chen, Fudan University, CN Jiangnan Yu, Hong Kong University of Science and Technology, CN
- **Hypnos: Memory Efficient Homomorphic Processing Unit**
  Haoxuan Wang, Yinghao Yang, Hang Lu, Xiaowei Li, Chinese Academy of Sciences, CN
- **GS-TG: 3D Gaussian Splatting Accelerator With Tile Grouping for Reducing Redundant Sorting While Preserving Rasterization Efficiency**
  Joongho Jo, Jongsun Park, Korea University, KR
- **BEVSA: A Real-Time Bird's-Eye-View Semantic Segmentation Accelerator for Multi-Camera System**
  Sangho Lee, Jueun Jung, Wuyoung Jang, Jihyeon Hwang, Kyuho Lee, Ulsan National Institute of Science and Technology (UNIST), KR
- **An Energy-Efficient Kalman Filter Architecture with Tunable Accuracy for Brain-Computer Interfaces**
  Guy Eichler, Joseph Zuckerman, Luca Carloni, Columbia University, US

Session Chair(s): Amir Fakhim Babaei, Virginia Tech; Ganapati Bhat, Washington State University

WATTS UP? AI/ML ENABLED ADVANCES IN POWER AND THERMAL INTEGRITY

Time: 3:30 PM - 5:30 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3006, Level 3

Description: Rising energy levels in modern chipsets due to larger computing workloads challenge the chip power integrity and have necessitated an efficient power analysis and a deeper exploration of methodologies to lower the overall power utilization. In light of these developments, this session presents novel techniques to estimate various attributes including IR drops, power-delivery networks, Place and Route, thermal analysis, and architectural enhancements. Furthermore, these works utilize novel AI/ML modeling and design automation approaches to optimize the design and EDA flow.

- **A Cutting-Edge Parallel Solver for Scalable Power Grid Analysis Using Nested Domain Decomposition**
  Jianfei Song, Cheng Zhuo, Zhejiang University, CN; Xiaoyu Yang, Zhou Jin, University of Petroleum, Beijing, CN
- **IRGNN: A Graph-Based Framework Integrating Numerical Solution and Point Cloud for Static IR Drop Prediction**
  Feng Guo, Yueyue Xi, Jianwang Zhai, Jingyu Jia, Jiawei Liu, Kang Zhao, Chuan Shi, Beijing University of Posts and Telecommunications, CN
- **LMM-IR: Large-Scale Netlist-Aware Multimodal Framework for Static IR-Drop Prediction**
  Kai Ma, Zhen Wang, Hongquan He, Hao Geng, ShanghaiTech University, CN; Qi Xu, University of Science and Technology of China, CN; Tinghuan Chen, The Chinese University of Hong Kong, Shenzhen, CN
- **Power-Grid Structure Exploration with Unified Sequence-Based Learning Framework**
  Yi-Lin Chuang, Hao-Wei Chan, Chih-Yun Yen, Shih-An Hsieh, Ching-Feng Chen, Sheng-Te Lai, MediaTek Inc., TW
- **Real-Time Dynamic IR-Drop Prediction for IR ECO**
  Yu-Che Lee, Yu-Hsuan Chen, Yu-Chen Cheng, Yi-Ting Li, Wuqian Tang, Shih-Chieh Chang, Chun-Yao Wang, National Tsing Hua University, TW; Yong-Fong Chang, Jia Wei Lin, Hsun-Wei Pao, Mediatek Inc, TW; Yung-Chih Chen, National Taiwan University of Science and Technology, TW
- **ATLAS: A Self-Supervised and Cross-Stage Netlist Power Model for Fine-Grained Time-Based Layout Power Analysis**
  Wenkai LI, Yao Lu, Wenji Fang, Jing WANG, Qijun Zhang, Zhiyao Xie, Hong Kong University of Science and Technology (HKUST), HK
- **NeuralMesh: Neural Network For FEM Mesh Generation in 2.5D/3D Chiplet Thermal Simulation**
  Pengju Chen, Dan Niu, Dekang Zhang, Southeast University, CN; Wenhao Wang, ShanghaiTech University, CN; Depeng Xie, BTD Technology, Inc, CN; Zhou Jin, University of Petroleum, Beijing, CN; Wei Xing, The University of Sheffield, GB; Lei He, University of California, Los Angeles, US
- **ASRR-PINN: Adaptive Sub-Regional Random Resampling-Based PINN for Thermal Analysis of 3D-ICs**
  Zijian Zhou, Min Tang, Shanghai Jiao Tong University, CN; Liang Chen, Shanghai University, CN

Session Chair(s): Prabal Basu, Cadence Design Systems, Inc.; Noel Daniel Gundi, Utah State University

MATERIALS TO SYSTEMS DESIGN AUTOMATION FOR ADVANCED CHIPS

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: We present four talks which delve into the entire semiconductor innovation process, from materials discovery to system-level design automation. It highlights how AI/ML methodologies and advanced simulation platforms can accelerate each step, addressing the complexities of modern semiconductor design. The discussion of high-bandwidth photonic interconnects, thermal-stress simulations and comprehensive EDA platforms underscore the transformative potential of integrating AI/ML into the semiconductor design workflow, ultimately leading to more efficient and powerful advanced chips.

- **Materials-Device-Systems Co-Optimization Using AI/ML**
  Gaurav Thareja, Applied Materials, US
- **Scalable Heterogenous Photonic Design Automation**
  Jesse Lu, Spin Photonics, US
- **Multi-Scale Thermal-Mechanical Modeling of Advanced Chips**
  Connor McClellan, DeepSim, US
- **Enhancing Design Automation with AI and Quantum Algorithms for Chip Design**
  Dario Thober, Von Braun Labs, BR

Organizer(s): Asif Khan, Georgia Institute of Technology

DESIGN, DEVLEOP, DOMINATE: THE CHIPS ACT'S ROLE IN SEMICONDUCTOR INNOVATION

Time: 4:00 PM - 4:45 PM

Topic Area(s): EDA

Session Type: DAC Pavilion Panel

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Silicon design is complex and expensive with high penalties for iterations. From start to finish, chip implementation has teams of 100s to 1000s of Engineers, geographically distributed across multiple time zones, and spans multiple years of development time. A typical design process goes through 100s of tools in the front end (from concept to tape-out) and an equally excruciating process in the back end (from silicon to product release). Silicon development costs have skyrocketed with the shrinking geometries - from sub-hundred million to above $500 million.

The complexity and efficiency of Silicon design process has of course been constantly studied. Take for example this survey conducted by Siemens & Wilson Research, which presents a study on Functional Verification. Functional verification has been a key focus for the industry - EDA leaders such as Synopsys, Cadence and Siemens have produced state of the art verification tools.

More recently, Nvidia has demonstrated that use of GenAI can bring significant efficiencies to the Silicon design process.

While there is heavy focus on productivity improvements in specific areas of Silicon Design, the question that remains is what can be done to make the entire design process more efficient. Needless to say, improving efficiency has a significant impact on the industry as a whole - it can reduce the time to market and enable the industry to produce more silicon, faster and cheaper... and this can be a winner for the whole tech industry as Silicon is at the foundation of all technology driving the AI revolution!

Silicon & Hardware Systems designs have significant similarities in process and efficiency challenges. Most people find the HW Systems design to be an extension of the process used in Silicon design making solutions for efficiency mutually beneficial.

Moderator: Bernard Murphy, SemiWiki, US

Panelists: Vidya Rajagopalan, Rivian, US; Rajesh Kashyap, Ericsson, US; Gopal Iyer, Lattice Semiconductor; Amit Dhir, PWC

A CONFIGURABLE ECAD LIBRARY SOLUTION FOR ALL USERS

Time: 4:15 PM - 4:45 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: In today's industry, component providers and semiconductor companies supply components to customers along with specification datasheets in PDF format. Product design and manufacturing companies (ODMs and OEMs) need to create their own component libraries to meet specific design and manufacturing requirements. In Recognizing this need, many component suppliers have started offering generic ECAD libraries to facilitate faster design integration.

However, creating ready-to-use ECAD libraries for everyone remains a challenge. Different ODMs and OEMs have varying design requirements, and manufacturers' capabilities and limitations also differ, which affects Design for Manufacturing (DFM) standards. As a result, engineers must customize the libraries to accommodate DFM adjustments to ensure that designs are both manufacturable and reliable.

Moreover, even within a single company, ideal component libraries must be easily updated whenever design rules or contract manufacturing conditions change. Companies often employ dedicated engineering team to handle such challenges.

Last year, when we presented at the DAC Exhibitor Forum, we discussed key technologies for building an accurate and reusable ECAD library platform. Since then, we have made exciting advancements.

As the industry starting to adopt these technologies, a major challenge getting engineers to adopt automated library design tools is ensuring that these tools feel as intuitive and adaptable as human designers. The ability to accept specific requirements and generate customized libraries accordingly is crucial. Yet, how to design an automated library platform with efficient yet flexible human-machine interaction that meets all design needs is a topic that has been largely overlooked in the industry.

Over the past year, we have made significant progress in this area and want to share our insights with the industry. We believe this is one of the most relevant topics for engineers today, as using AI and automation tools in their work will become a norm. We've developed an integrated ECAD library system that, at its core, digitizes the entire design-for-manufacturing knowledge base and library creation process. This system opens APIs that allow users to flexibly embed any chosen DFM aspects into their libraries. It enables users to set their own DFM rule parameters and instantly receive library files that adhere to their specific design requirements in their preferred EDA format.

The goal is to share our experience, shed light on the real challenges the industry faces in adopting AI and automation tools, and help alleviate the burden of the cumbersome library-building process. By doing so, we aim to transform the industry, enabling companies to allocate engineering resources to the more creative aspects of design; Additionally, we aim to encourage component suppliers to provide digital datasheets or ready-to-use digital libraries, which will not only benefit the industry but also align with the broader trend toward digitization.

Speaker: Julie Liu, Palpilot International, US

POWERING AI INFRASTRUCTURE WITH INNOVATIONS IN RELIABLE IN SYSTEM/ON-DIE MEMORY DESIGN AND CHARACTERIZATION

Time: 5:00 PM - 5:30 PM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Driven by the frantic pace of Large Language Model adoption, AI is dramatically redefining Data Center Infrastructure requirements. For instance, Meta's Llama 3 needed 16,000 Nvidia Hopper GPUs and 70 days to train, negotiating 405 Billion parameters and using 15.6 Trillion tokens. Such massive workloads demand not only optimally fast interconnects and innovations in Power delivery, but they also demand materially superior design and reliability performance from Compute's eternal execution twin - Memory, both on and off chip. Memory requirements for High Performance compute are an increasing challenge as new versions of LLMs (eg. Llama 3.1) are pushing per-model-instance memory requirements to nearly a Terabyte (854 GB to be precise), which in turn means subsequent generations of GPUs (like the H200) and other general purpose SoCs will have to support significantly larger on-die Memory clusters. Designing, characterizing and delivering reliable Memory banks within acceptable time-to-market windows thus becomes a key competency that deserves increasing focus. Our design team's track record of delivering multiple generations of silicon proven Memory IP in the most advanced process nodes across multiple foundries and customers, enables us to be a significant part of that focus. Our design experience is enhanced by addressing advanced testability demands of modern multi-die SOCs, including proven history of designing on-chip memory diagnostics (to enable real-time fault monitoring without need for external testers), supporting pattern diagnosis, debug, flexible repair hierarchies and Quality of results optimization, all techniques for non-intrusive fault tolerance and optimal system performance essential for AI/ML applications.

Double-click on our expertise and you will find Infosys employing robust AI/ML powered algorithms in the Memory design and characterization process. Using these algorithms, we are identifying critical paths within large memory instances, predicting PPA metrics across different process, voltage and temperature corners and aging corners efficiently. These techniques dramatically reduce memory design times by eliminating the need to run actual simulations across all corners. Any design/feature change requires re-characterization and model retraining ONLY over the corresponding leaf cell(s) while complier range change does not require any further adjustments. Such innovations, using AI to power development of future AI platforms, is one of many reasons why Infosys is a dependable partner in delivering core (Silicon) elements of AI infrastructure.

Speakers: Ehsan Rashid, Chetan Kumar, Shreekanth

POSTER GLADIATOR BATTLE

Time: 5:00 PM - 6:00 PM

Session Type: Monday Poster Gladiator Battle

Room: DAC Pavilion, Level 2 Exhibit Hall

MONDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 5:00 PM - 6:00 PM

Session Type: Engineering Poster

Room: Engineering Posters, Level 2 Exhibit Hall

3D-IC HETEROGENEOUS SYSTEM IMPLEMENTATION USING VIRTUOSO STUDIO AND INTEGRITY SYSTEM PLANNER

Gourav Uppal, Amit Kumar, Hitesh Marwah, Chayan Majumder, Dan Baldwin, Cadence Design Systems, Inc., US

A CONSTRUCTIVE APPROACH TO LEFT-SHIFT PRELIMINARY IDENTIFICATION OF CRITICAL SILICON BREAKING ANOMALIES

Ayushi Bapna, Arif Mohammed, Texas Instruments, IN

A NEW METHODOLOGY TO GENERATE A MULTITUDE OF SOC CONFIGURATIONS QUICKLY

Fernand Da Fonseca, Arm Ltd., US; Chouki Aktouf, Valentin Boyer, Mael Rabe, Defacto Technologies, FR

A NOVEL APPROACH FOR LOGIC EQUIVALENCE CHECK AFTER PIPELINE RETIMING IN ECO

Naveen Bishnoi, Sardar Bhukya, Mohit Rawat, Sneha Biswas, Satish Sethuraman, Nilabh Srivastava, Intel Corporation, IN Bassilios Petrakis, Cadence Design Systems, Inc., US

MONDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

A NOVEL TEST POINT INSERTION METHODOLOGY FOR ENHANCED TEST EFFICIENCY AND IMPROVED DESIGN QUALITY
Pervez Garg, Piyushkumar Chaniyara, Texas Instruments, IN

A PCA AND KDE BASED APPROACH FOR STATISTICAL CMOS COMPACT MODEL PARAMETER GENERATION
Yifan Zhou, Xuge Fan, Jie Ding, Beijing Institute of Technology, CN; Asen Asenov, University of Glasgow, GB

A SAFETY CENTRIC APPROACH TO FUNCTIONAL VERIFICATION OF DUAL CORE LOCK-STEP DESIGNS
Mohammad Rashid, Suharini C, Ratan Deep, Harsh Setia, Samsung Semiconductor, IN

ACCELERATING SYSTEM VALIDATION USING EMULATION AND FPGA PROTOTYPING PLATFORMS
Ponnambalam Lakshmanan, Ajeet Mall, Analog Devices, Inc. (ADI), IN

ACTIVE DEVICE TESTKEYS ENABLE FEOL-PROCESS MONITORING AND PERFORMANCE IMPROVEMENT
Zhikun Liu, Xiaochuan Wang, Kun Zhou, Jian Wang, Guohua Zhou, Keqing Ouyang, Sanechips Technology Co., Ltd, CN

ADVANCED APL MODELING METHOD FOR COMPLEX I/O BUFFER DESIGNS FOR ACCURATE SOC IR DROP ANALYSIS
Jean FrancoisAnil Dwivedi, Atul Bhargava, Ankur Bal, STMicroelectronics, IN

ADVANCED YIELD PREDICTION FOR SRAM BITCELLS WITH RARE DEFECT MODELING LEVERAGING AI-POWERED METHODOLOGY
Mohamed Atoua, Siemens, US; Sandeep Puri, GlobalFoundries, US

AI/ML DRIVEN OPTIMIZATION FOR EFFICIENT ATPG IN LARGE SCALE DESIGNS
Pervez Garg, Piyushkumar Chaniyara, Satish Sajjanar, Texas Instruments, IN

AN EFFICIENT METHODOLOGY OF ANALYZING RUSH CURRENT IN POWER GATED DESIGN
Abhinav Gaur, Akhilesh Mishra, NXP, IN; Ankur Chavhan, Cadence Design Systems, Inc., IN

AUTOMATED AI-ML BASED FLOW FOR VALIDATED CONSTRAINT GENERATION FOR CDC/RDC
Abdul Moyeen, Siemens, US

AUTOMATED IR CONVERGENCE WITH PRIMECLOSURE IR-ECO
Shreya Mysore Panduranga, Hailang Wang, Jimmy Wu, Piyush Jain, Rossana Liu, Srinivasulu M, Synopsys, US

AUTOMATED IR-ECO FLOW: REDUCING PDN VIOLATIONS UPTO 40-50% AND SAVING WEEKS OF ENGINEERING EFFORT
Mohit Jain, Qualcomm, US; Roshan Roy, Ansys, US; Len Hsu, Synopsys, TW

AUTOMATED "SPEC TO SIGN-OFF" OF CSR AND INTEGRATION VERIFICATION AT SOC
Sai Nikhil Kandukuri, Presidency University Bangalore, IN; Swathi Nagarajasetty, Visvesvaraya Technological University, IN; Sunil Kashide, Samsung Semiconductor, IN; Garima Srivastava, Vijaya Gupta, Gopikrishna Kommidi, Samsung, IN

CHIP PACKAGE LEVEL THERMAL INTEGRITY ANALYSIS OF HIGH-POWER DATA CENTER CHIPS FOR HOT SPOT DETECTION
Sumanth Suraneni, Annapurna Labs US Inc., US; Nikhil Jayakumar, Amazon, US; Sujyesh Aanandh Manjunthan, Ansys, US

CIRCUIT DESIGN AND OPTIMIZATION METHODOLOGY ENSURING AREA OPTIMIZED, ROBUST AND RELIABLE I/O INTERFACE FOR WIDE RANGE OF APPLICATION USE
Anuj Gupta, Suprbha Kumari, Anil Dwivedi, STMicroelectronics, IN

COMPREHENSIVE SOLUTION FOR OPTIMIZING AND ACCELERATING GATE LEVEL SIMULATION FOR COMPLEX SOCS
Pradeep Sahoo, Sunil Kashide, Garima Srivastava, Narasimha Chinni, Shekhar Sharma, Prem Sinha, Samsung, IN

CONGESTION FREE, POWER DOMAIN AWARE SIGNAL MULTIPLEXING
Dinesh Joshi, Nidhi Sinha, NXP Semiconductors, IN

DESIGN FLOORPLAN-DRIVEN LOCALIZATION OF SMS PROCESSORS FOR OPTIMIZED MEMORY PERFORMANCE
A S Ramkumar Reddy, Lakshmi Sarvaani Pallapu, R Santhosh Kumar, Anil Kumar Ede, Intel Corporation, US

DESIGN OPTIMIZATION OF ASIC DESIGNS VIA AI-DRIVEN RTL-TO-GDS OPTIMIZATION WITH FLOORPLANNING
Jennifer Kazda, Wachirawit Ponghiran, Derren Dunn, IBM, US; Anindita Gangwar, Ben Beaumont, Cadence Design Systems, Inc., US

ENHANCED LVS TECHNIQUES FOR FAST CONVERGENCE AND OPTIMIZED DESIGN CYCLES
Vandana Narula, Ertugrul Demircan, NXP Semiconductors, US; Gazal Singla, Siemens, IN

ENHANCING TIMING CLOSURE IN HIGH-FREQUENCY DESIGNS THROUGH PRECISE LATENCY CONTROL AND TIMING-AWARE SINK ASSIGNMENT
Naveen Bishnoi, Roopa Tigadi, Nilabh Srivastava, Intel Corporation, IN; Kishan Ramesh, Gowry Sankar, Cadence Design Systems, Inc., IN

MONDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

ENSURING DRAM COMPLIANCE: NOVEL VERIFICATION TECHNIQUES FOR REFRESH AND REFRESH MANAGEMENT IN MODERN DRAM ARCHITECTURE
Shyam Sharma, Gruheshkumar Patel, Dharini Subashchandran, Cadence Design Systems, Inc., IN

EXPEDITING CUSTOM CORE SOC VERIFICATION AND COVERAGE DRIVEN FIRMWARE SIGN-OFF USING ESWD & VERISIUM DEBUG
Ayushi Bapna, Arif Mohammed, Yogeshwaran Shanmugam, Ashwini Padoor, Texas Instruments, IN

FAST-TRACKING PCIE VERIFICATION IN AN SOC BY AUTOMATING THE TESTBENCH USING TRIPLE CHECK TEST-SUITE
Subramanian R, Sekhar Dangudubiyyam, Naga Swetha Maddulapalli, Samsung Semiconductor, IN

GENERATIVE AI FOR IMPROVING THE PRODUCTIVITY IN ANALOG & MIXED SIGNAL DESIGN FLOWS
Nupur Bhonge, Amazon, US; Prathna Sekar, Keysight Technologies, US

HBM TIMING METHODOLOGY WITH LIBERTY LVF
Eric Hsu, Ying Luo, Nvidia, US; An-Jui Shey, Empyrean Technology, US

HIERARCHICAL EM-IR SIGNOFF METHODOLOGY FOR LARGE SOCS INTEGRATED IN 2.5DIC STRUCTURES
Sumanth Suraneni, Annapurna Labs US Inc., US; Nikhil Jayakumar, Amazon, US; Maryam Moradpour, Ansys, CA; Ansh Dudeja, Ansys, IN

HIGH-CAPACITY, HIGH-PERFORMANCE CHIP-LEVEL ESD ANALYSIS FOR RELIABLE SEMICONDUCTOR DESIGNS
Vinoth Murugesan, Qualcomm, US; Kumar Avala, Ansys, US

INTERCONNECTION TESTKEYS ENABLE BEOL-PROCESS MONITORING AND RC ACCURACY IMPROVEMENT
Kun Zhou, Jian Wang, Zhikun Liu, Xiaochuan Wang, Guohua Zhou, Keqing Ouyang, Sanechips Technology Co.,Ltd, CN

INTEGRATING SELF-HEAT ANALYSIS IN MULTIPHYSICS SIMULATION FOR ADVANCED SEMICONDUCTOR CHIP DESIGN
Stuti Singh, Ansys, IN; Pritesh Johari, Arian Fanaian, Qualcomm, US

IR-AWARE TIMING ANALYSIS USING ACCURATE DVD-PWL FLOW FOR ADVANCED TECHNOLOGY NODES
Rajnish Garg, Anil Yadav, STMicroelectronics, IN

LEVERAGING MACHINE LEARNING TO AUTOMATE WAIVER GENERATION FOR STATIC LINT VIOLATIONS
Mohan Mangal, Himanshu Kathuria, Jaskaran Ajimal, Synopsys, US

MACHINE LEARNING BASED LAYOUT OPTIMIZATION OF ELECTROMAGNETIC STRUCTURES FOR HIGH-SPEED IO DESIGN
Garth Sundberg, Ansys, US

MCP INDUCED GLITCHES
Dinesh Joshi, Nidhi Sinha, NXP Semiconductors, IN

METHOD & APPARATUS TO MIGRATE DESIGN REPOSITORIES INTO CLOUD
Nupur Bhonge, Amazon, US; Prathna Sekar, Keysight Technologies, US

METHOD OF CONSTRAINT TRANSFORMATION IN STATIC TIMING ANALYSIS FOR DUAL EDGE TIMING
Jack DiLullo, Eric Foreman, Manish Verma, IBM, IN

METHODOLOGY TO GENERATE SYNTHESIS SIGNOFF QUALITY OPTIMIZED REGISTERS AT RTL AND APPLICATION OF GENERATED OPTIMIZED REGISTERS INTO RTL AND IMPLEMENTATION DESIGN FLOWS TO IMPROVE PRODUCTIVITY
Suresh Barla, Bhavana Mallikarjunaiah, Himanshu Kathuria, Jaskaran Ajimal, Synopsys, US

OPTIMIZING NETWORK STORAGE FOR AI-POWERED EDA DEPLOYMENTS
Prathna Sekar, Keysight Technologies, US

OPTIMIZING POWER INTEGRITY WITH SMART PDN FRAMEWORK
Gaurav Jain, Rajender Nune, Vinay Kumar B U, Srihari Darapu, Qualcomm, IN

"OPTIMIZING TIMING CONVERGENCE IN HIGH-SPEED PCIE SYSTEMS: AN EDA METHODOLOGICAL APPROACH"
Keshavkumar Durgakeri, Anilkumar Ede, A Subbaramkumar Reddy, Saidesh Pasupuleti, Intel Corporation, IN

PPA FRIENDLY CUSTOM REPEATER TREE INSERTION FOR HIGH-SPEED DESIGNS
Sachin Mirajkar, Sarala Gumma, Intel, IN

REAL-TIME PROCESS MARGIN-BASED LAYOUT OPTIMIZATION
Collin Tranter, Navneet Jain, Romain Feuillette, David Pritchard, Heather Lazar, Nolan Pavek, Stephen Burgess, Benoit Ramadout, GlobalFoundries, DE

REUSABLE AND EFFICIENT SCOREBOARD IMPLEMENTATION FOR BUG HUNTING AND TESTBENCH PRODUCTIVITY
Sougata Bhattacharjee, Gulshan Sharma, Guru Chapi, Samsung Semiconductor, IN

REVOLUTIONISING SOC VERIFICATION THROUGH SYSTEM VERILOG EENET-ENHANCED BEHAVIOURAL MODEL FOR PRECISION IN ANALOG IP CHARACTERISATION
Aadhar Sharma, Sooraj Sekhar, Lakshmanan Balasubramanian, Bhavya Shah, Avinash Chaudhary, Texas Instruments, IN; Stefan Dannenberger, Texas Instruments, NO

MONDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

SOLVING CONFIGURATION CHALLENGE WITH SVRAND VERIFICATION FLOW
Krunal Kapadiya, Kaushal Vala, Joseph Bauer, Shyam Sharma, Cadence Design Systems, Inc., US

SPREADSHEET AUTOMATA: A SYSTEMATIC APPROACH TO EXECUTING SPREADSHEET STATE MACHINES IN C++ PERFORMANCE MODELS
Zachary Ankenman, Biju Puthur Simon, Ramesh Krishna Jayaraman, OpenEdges, US

STREAMLINED RTL CLOCK MANAGEMENT: A PYTHON FRAMEWORK FOR CLOCK TRACING, CLOCK SPEC VERIFICATION AND STA CONSTRAINT GENERATION
Tejas Salunkhe, Faeq Hussain, Texas Instruments, IN

TIMING-AWARE SMART PG FILL
Rahul Pandey, Anil Yadav, Biswarup Pal, Davinder Aggarwal, STMicroelectronics, IN Ankur Chavhan, Cadence Design Systems, Inc., IN

USING AI TO VALIDATE STANDARD CELL LIBERTY IP RIDDLED WITH SPARSE AND DISPARATE DATA
Ray Valencia, Siemens, CA; Ajay Kumar, Siemens, GB; Aravind Radhakrishnan Nair, Infineon, DE

USING BIG DATA AND ML TECHNIQUES TO TRIAGE TIMING VIOLATIONS
Lukas Pettersson, Marvell, US

MONDAY LATE BREAKING RESULTS POSTER RECEPTION

Time: 6:00 PM - 7:00 PM

Session Type: Late Breaking Results Poster

Room: Level 2 Lobby

LATE BREAKING RESULTS: A DIFFUSION-BASED FRAMEWORK FOR CONFIGURABLE AND REALISTIC MULTI-STORAGE TRACE GENERATION
Seohyun Kim, Junyoung Lee, Jongho Park, Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, KR; Jinhyung Koo, Sungjin Lee, Pohang University of Science and Technology (POSTECH), KR

LATE BREAKING RESULTS: A FAST NEAREST NEIGHBOR SEARCH ACCELERATION FOR 3D POINT CLOUD
Jinao Li, Qianyu Cheng, Zhendong Zheng, Lei Gong, Chao Wang, Xi Li, Xuehai Zhou, University of Science and Technology of China, CN

LATE BREAKING RESULTS: A GEOMETRIC DIFFUSION MODEL FOR MACRO PLACEMENT GENERATION
Jongho Yoon, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), KR; Jinsung Jeon, University of California, San Diego, US

LATE BREAKING RESULTS: ADVANCED PCB PLACEMENT WITH IRREGULAR COMPONENTS FOR EFFICIENT COLLISION DETECTION AND ROUTABILITY OPTIMIZATION
Chien-Hao Tsou, Zhu-Xun Lee, Yao-Wen Chang, National Taiwan University, TW

LATE BREAKING RESULTS: AN EFFICIENT AND SCALABLE TRACK ASSIGNMENT WITH GPU PARALLELISM
Genggeng Liu, Pengcheng Huang, Zepeng Li, Wenzhong Guo, Fuzhou University, CN; Wen-Hao Liu, Nvidia, TW; Xing Huang, Northwestern Polytechnical University, CN

LATE BREAKING RESULTS: AUTOMATED TOPOLOGY GENERATION FOR POWER AMPLIFIER DESIGNS THROUGH BILSTM-BASED DNN AND MULTI-OBJECTIVE OPTIMIZATIONS
Lida Kouhalvandi, Dogus University, TR; Sercan Aygun, University of Louisiana, Lafayette, US; M. Hassan Najafi, Case Western Reserve University, US; Arman Roohi, University of Illinois, Chicago, US

LATE BREAKING RESULTS: BLAST: BISECTION-FREE LEARNING APPROACH FOR STATISTICAL TIMING CHARACTERIZATION
Kai Jing, Tao Bai, Zeyuan Deng, Junming Jiao, Peng Cao, Southeast University, CN

LATE BREAKING RESULTS: BREAKING SYMMETRY---UNCONVENTIONAL PLACEMENT OF ANALOG CIRCUITS USING MULTI-LEVEL MULTI-AGENT REINFORCEMENT LEARNING
Supriyo Maji, Linran Zhao, Souradip Poddar, David Pan, The University of Texas at Austin, US

LATE BREAKING RESULTS: CUSTOMIZED DIFFUSION MODEL EMPOWERED BY HETEROGENEOUS GRAPH NETWORK FOR EFFECTIVE FLOORPLANNING
Xinglin Zheng, Hao Gu, Keyu Peng, Youwen Wang, Wenxing Zhu, Ziran Zhu, Southeast University, US

LATE BREAKING RESULTS: DECENTRALIZED VOTING-BASED ATTESTATION FOR IOT DEVICES
Mohamed Alsharkawy, Eren Sönmez, Jeferson Gonzalez-Gomez, Hassan Nassar, Joerg Henkel, Karlsruhe Institute of Technology, DE

LATE BREAKING RESULTS: ENCODER-DECODER GENERATIVE DIFFUSION TRANSFORMER TOWARDS PUSH-BUTTON ANALOG IC SIZING
Filipe Azevedo, Nuno Lourenco, Ricardo Martins, Universidade de Lisboa, PT

LATE BREAKING RESULTS: FINE-TUNING LLMS FOR TEST STIMULI GENERATION
Hyeonwoo Park, Seonghyeon Park, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), KR

LATE BREAKING RESULTS: FPGEN-3D: AUTOMATED FRAMEWORK FOR 3D-FPGA ARCHITECTURE GENERATION AND EXPLORATION
Ismael Youssef, Cong "Callie" Hao, Georgia Institute of Technology, US

MONDAY LATE BREAKING RESULTS POSTER RECEPTION (continued)

LATE BREAKING RESULTS: HYBRID LOGIC OPTIMIZATION WITH PREDICTIVE SELF-SUPERVISION

Rongliang Fu, Ziyang Zheng, Zhengyuan Shi, Yuan Pu, Qiang Xu, Tsung-Yi Ho, The Chinese University of Hong Kong, HK; Ran Zhang, Junying Huang, Institute of Computing Technology, Chinese Academy of Sciences, CN

LATE BREAKING RESULTS: IN-MEMORY ARITHMETIC: ENABLING DIVISION WITH STOCHASTIC LOGIC

Farzad Razi, Marc Riedel, University of Minnesota, US; Mehran Shoushtari Moghadam, M. Hassan Najafi, Case Western Reserve University, US; Sercan Aygun, University of Louisiana, Lafayette, US

LATE BREAKING RESULTS: LESS SENSE MAKES MORE SENSE: IN-SENSOR COMPRESSIVE LEARNING FOR EFFICIENT MACHINE VISION

Yiwen Liang, Weidong Cao, George Washington University, US

LATE BREAKING RESULTS: MULTI-OBJECTIVE MULTI-BIT FLIP-FLOP PLACEMENT CONSIDERING PRE-PLACED CELLS

Cheng-Yen Li, Chuan-Chi Su, Zheng-Wei Chen, Shao-Hsiang Chen, Yao-Wen Chang, National Taiwan University, TW

LATE BREAKING RESULTS: NOVEL DESIGN OF MTJ-BASED UNIFIED LIF SPIKING NEURON AND PUF

Milad Tanavardi Nasab, Wu Yang, Himanshu Thapliyal, University of Tennessee, Knoxville, US

LATE BREAKING RESULTS: ON-THE-FLY HADAMARD HYPERVECTOR PROCESSING FOR EFFICIENT HYPERDIMENSIONAL COMPUTING

Abu Kaiser Mohammad Masum, Sercan Aygun, University of Louisiana, Lafayette, US: Shoushtari Moghadam, M. Hassan Najafi, Case Western Reserve University, US; Sabrina Hassan Moon, Ahmed Mamdouh, Dayane Reis, University of South Florida, US

LATE BREAKING RESULTS: OPERA: AN OPEN AND EFFICIENT PLATFORM FOR DATA-DRIVEN SYNTHESIS OF ANALOG CIRCUITS

Shikai Wang, Zhiqiang Yi, Weidong Cao, George Washington University, US; Yaolong Hu, Taiyun Chi, Rice University, US

LATE BREAKING RESULTS: SCALABLE GPU-FRIENDLY PARALLELIZATION FOR SWEEP-BASED MAZE ROUTING

Cheng-Yu Chiang, Zong-Ying Cai, Chao-Chi Lan, Yan-Jen Chen, Yang Hsu, Yao-Wen Chang, National Taiwan University, TW; Hung-Ming Chen, National Yang Ming Chiao Tung University, TW

LATE BREAKING RESULTS: SOURCE-AWARE ADAPTIVE CACHE MANAGEMENT FOR CXL-ENABLED DISAGGREGATED MEMORY SHARING

Qianyu Cheng, JiaJun Ji, Teng Wang, Zihan Wang, Lei Gong, Chao Wang, Xuehai Zhou, University of Science and Technology of China, CN

LATE BREAKING RESULTS: STATISTICAL TIMING GRAPH SCHEDULING ALGORITHM FOR GPU COMPUTATION

Chih-Chun Chang, Tsung-Wei Huang, University of Wisconsin, Madison, US

LATE BREAKING RESULTS: THE HIDDEN RISKS OF ACTIVATION DURATION IN PLPUFS

Mohamen Alsharkawy, Jan Zwerschke, Hassan Nassar, Jeferson Gonzalez-Gomez, Joerg Henkel, Karlsruhe Institute of Technology, DE

LATE BREAKING RESULTS: UTILIZATION OF HYBRID THRESHOLD-VOLTAGE FLIP-FLOPS FOR POWER RECOVERY

Sehyeon Chung, Taewhan Kim, Seoul National University, KR; Hyunchul Hwang, Byungsu Kim, Jaeha Lee, Kunhyuk Kang, Samsung, KR

LATE BREAKING RESULTS: VERSATILE 4:1 MULTIPLEXER USING 1T1R RRAM CROSSBAR FOR HIGH SPEED IN-MEMORY COMPUTING

Vinod Kumar, Binsu Kailath

LATE BREAKING RESULTS: WARPAGE-AWARE GENERATIVE FLOORPLANNING FOR RELIABLE ADVANCED PACKAGING

Min-Hung Chen, Cheng-Yen Li, Chuan-Chi Su, Yao-Wen Chang, National Taiwan University, TW; Tung-Chieh Chen, Synopsys, TW

MONDAY WORK-IN-PROGRESS POSTER RECEPTION

Time: 6:00 PM - 7:00 PM

Session Type: Work-in-Progress Poster

Room: Level 2 Lobby

A NOVEL MULTI-NODE-UPSET RECOVERABILITY VERIFICATION METHOD WITH GENERALIZED MODEL FOR RADIATION-HARDENED LATCHES

Aibin Yan, Hefei University of Technology, CN; Yongkang Xu, Hefei University of Technology, CN; Wangjin Jiang, Hefei University of Technology, CN; Zhengfeng Huang, Hefei University of Technology, CN; Tianming Ni, Anhui Polytechnic University, CN; Xiaoqing Wen, Kyushu Institute of Technology, JP; Patrick Girard, LIRMM / CNRS, FR; Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, CN

A NOVEL POWER-GRADIENT-AWARE CELL PLACEMENT METHODOLOGY CONSIDERING 3D-IC STACKING THERMAL BOUNDARY TO ACHIEVE TIMING AND THERMAL CO-OPTIMIZATION

Chien-Chih Huang, Intel Foundry, TW; Ming-Chuan Hu, Intel Foundry, TW; Po-Hsiang Huang, Intel Foundry, TW; Wei-Yi Hu, Intel Foundry, US

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

ACCELERATING IC THERMAL SIMULATION DATA GENERATION VIA BLOCK KRYLOV AND OPERATOR ACTION

Hong Wang, University of Science and Technology of China, CN; Wenkai Yang, ShanghaiTech University, CN; Jie Wang, University of Science and Technology of China, CN; Huanshuo Dong, University of Science and Technology of China, CN; Zijie Geng, University of Science and Technology of China, CN; Zhen Huang, University of Science and Technology of China;Eastern Institute of Technology, CN; Depeng Xie, Southeast University, CN

ADDRESSING SEQUENTIAL CONSTRAINTS IN ZONED STORAGE WITH COLLECTIVE LOG-STRUCTURED FILE SYSTEM

Chang-Gyu Lee, Sogang University, KR; Youngjae Kim, Sogang University, KR

ADEM: ACCELERATING SPARSE MATRIX MULTIPLICATION WITH ADAPTIVE DATAFLOW AND EFFICIENT MERGING

Luo shengbai, National University of Denfense Technology, CN; Bo Wang, National University of Denfense Technology, CN; Yihao Shi, National University of Defence Technology, CN; Yuhan Tang, National University of Defense Technology, CN; Qingshan Xue, National University of Defense Technology, CN; Xueyi Zhang, National University of Defense Technology, CN; Yunping Zhao, National University of Defense Technology, CN; Sheng ma, National University of Defense Technology, CN; Tiejun Li, National University of Defense Technology, CN

ADVANCED DETECTION OF HARDWARE TROJANS IN POST-LAYOUT ICS: A GDSII-FOCUSED METHODOLOGY

Yaroslav Popryho, UIC, US; Inna Partin-Vaisband, University of Illinois at Chicago, US

AN EFFICIENT WEAR-LEVELING-AWARE PARALLEL ALLOCATOR FOR MULTIPLE PERSISTENT MEMORY FILE SYSTEMS

Ting Wu, Nanyang Technological University, CN; Linbo Long, Chongqing University, CN; Zhulin Ma, Chongqing University of Posts and Telecommunications, CN; Yulong Zhou, Chongqing University of Posts and Telecommunications, CN; Weichen Liu, Nanyang Technological University, SG

AN EXPERIENCE SHARING: A PANORAMIC-VISION LESION-FINDING LOW-POWER WIRELESS ENDOSCOPIC SYSTEM DESIGN AND IMPLEMENTATION

ching-hwa cheng, Feng-Chia University, TW

ANALYTICAL OPTIMIZATION FOR ROBUST AND EFFICIENT ANALOG IC DESIGN AUTOMATION

Alec Adair, The University of Utah, US; Armin Tajalli, The University of Utah, US

ANALYTICAL WARPAGE-AWARE MULTI-DIE FLOORPLANNING FOR ADVANCED PACKAGE DESIGNS

Shao-Yu Lo, National Taiwan University, TW; Min-Hung Chen, National Taiwan University, TW; Yao-Wen Chang, National Taiwan University, TW

BOOLEAN REASONING GUIDED UNGROUPING

Eleonora Testa, Synopsys Inc, US; Giulia Meuli, Synopsys, IT; Elena Teica, Synopsys Inc, US; Alan Vaz, Synopsys Inc, US; Vishal Aralikatti, Synopsys, IN; Abhishek Kumar, Synopsys, IN; Brian Lockyear, Synopsys, US; Luca Amaru, Synopsys Inc., US

CARBONEDA: CARBON-AWARE ELECTRONIC DESIGN AUTOMATION FOR INTEGRATED CIRCUITS

David Kong, Harvard University, US; Danielle Grey-Stewart, Harvard University, US; Mariam Elgamal, Harvard University, US; Gage Hills, Harvard University, US

CD2A: CONTINUOUS DEVICE-TO-DEVICE AUTHENTICATION EXPLOITING CRYSTAL OSCILLATOR IMPURITIES

muthupavithran selvam, student, GB; Zeba Khanam, BT Applied Research, GB; Amit Kumar Singh, University of Essex, GB; Zhan Cui, BT Applied Research, GB; Muttukrishnan Rajarajan, City University of London, GB

ACALSIM: A MULTI-THREADED SIMULATION FRAMEWORK FOR LARGE-SCALE PARALLEL SYSTEM DESIGN SPACE EXPLORATION

Wei-Fen Lin, TW High-Performance Education Association, TW; Zi-Yi Tai, Rivos Inc., US; Jen-Chien Chang, TW High-Performance Computing Education Association, TW; Yen-Po Chen, TW High-Performance Education Association, TW; Chia-Pao Chiang, TW High-Performance Education Association, TW; Yu-Yang Lee, National Cheng Kung University, TW; Yu-Jie Wang, TW High-Performance Education Association, TW; Ming-Der Hsieh, National Cheng Kung University, TW

CIRCUITSYNTH-RL: LLM-BASED CIRCUIT TOPOLOGY SYNTHESIS WITH RL REFINEMENT

Prashanth Vijayaraghavan, IBM Research, US; Luyao Shi, IBM Research, US; Ehsan Degan, IBM, US; Vandana Mukherjee, IBM, US; Xin Zhang, IBM, US

CONNAS4ML: CONSTRAINT-AWARE DIFFERENTIABLE NEURAL ARCHITECTURE SEARCH FOR EFFICIENT FPGA DEPLOYMENT

Chi-Jui Chen, National Yang Ming Chiao Tung University, TW; Bo-Cheng Lai, National Yang Ming Chiao Tung University, TW

CPCRFUZZ: CRITICAL PATH AND CONTROL REGISTER DIRECTED FUZZING FOR HARDWARE VULNERABILITY

Lei Peng, Harbin Institute of Technology, CN; Aijiao Cui, Harbin Institute of Technology, CN; Wei Zhang, Hong Kong University of Science and Technology (HKUST), HK; Gang Qu, University of Maryland College Park, US

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

CROSSTALK-AWARE MAPPING FOR OPTICAL NEURAL NETWORKS

Yuetong Fang, The Hong Kong University of Science and Technology (Guangzhou), CN; Ziqing Wang, Northwestern University, US; Renjing Xu, The Hong Kong University of Science and Technology (Guangzhou), CN

A HIGHLY ENERGY-EFFICIENT BINARY BERT MODEL ON GROUP VECTOR SYSTOLIC CIM ACCELERATOR

Dingbang Liu, Southern University of Science and Technology, CN; Ziyi Guan, The University of Hong Kong, HK; Qilong Chen, Southern University of Science and Technology, CN; Jiaqi Yang, Southern University of Science and Technology, CN; Kai Li, Southern University of Science and Technology, CN; Mingqiang Huang, Shenzhen Institutes of Advance Technology, CN; Changwen Chen, The Hong Kong Polytechnic University, HK; Ngai Wong, The University of Hong Kong, HK; Hao Yu, Southern University of Science and Technology, CN

DIREC: ENHANCING VHDL CODE GENERATION AND SUMMARIZATION WITH DIVIDE-RETRIEVE-CONQUER STRATEGY

Prashanth Vijayaraghavan, IBM Research, US; Apoorva Nitsure, IBM, US; Luyao Shi, IBM Research, US; Charles Mackin, IBM Research, US; Tyler Baldwin, IBM Research, US; David Beymer, IBM Research, US; Ehsan Degan, IBM, US; Vandana Mukherjee, IBM, US

DYGRASS: DYNAMIC SPECTRAL GRAPH SPARSIFICATION VIA LOCALIZED RANDOM WALKS ON GPUS

Yihang Yuan, Stevens Institute of Technology, US; Ali Aghdaei, Stevens Institute of Technology, US; Zhuo Feng, Stevens Institute of Technology, US

DYNA-OPTICS: ARCHITECTING A CHANNEL-ADAPTIVE DNN NEAR-SENSOR OPTICAL ACCELERATOR FOR DYNAMIC INFERENCE

Deniz Najafi, New Jersey Institute of Technology, US; Wanhao Yu, University of North Carolina at Charlotte, US; Mehrdad Morsali, New jersey Institute of Technology, US; Pietro Mercati, Intel, US; Mohsen Imani, University of California Irvine, US; Mahdi Nikdast, Colorado State University, US; li yang, University of North Carolina at Charlotte, US; Shaahin Angizi, New Jersey Institute of Technology, US

EFFICIENT EDGE AI LEARNING WITH EQUILIBRIUM PROPAGATION: A PRACTICAL SOLUTION FOR GRADIENT COMPUTATION

Mohamed Watfa, LIRMM / University of Montpellier 2, FR; Alberto Garcia-Ortiz, ITEM (U.Bremen), DE; Gilles Sassatelli, LIRMM CNRS / University of Montpellier 2, FR

EMAMBA: EFFICIENT ACCELERATION OF MAMBA MODELS FOR EDGE COMPUTING

Jiyong Kim, University of Ulsan, KR; Jaeho Lee, University of Ulsan, KR; Jiahao Lin, University of Wisconsin Madison, US; Alish Kanani, University of Wisconsin Madison, US; Umit Ogras, University of Wisconsin - Madison, US; Jaehyun Park, University of Ulsan, KR

ENHANCING LLMS FOR HDL CODE OPTIMIZATION USING DOMAIN KNOWLEDGE INJECTION

Che-Ming Chang, National Taiwan University, TW; Prashanth Vijayaraghavan, IBM Research, US; Charles Mackin, IBM Research, US; Ashutosh Jadhav, IBM, US; Hsinyu Tsai, IBM, US; Vandana Mukherjee, IBM Research, US; Ehsan Degan, IBM, US

A TENSOR-TRAIN DECOMPOSITION COMPRESSED LLMS ON GROUP VECTOR SYSTOLIC ACCELERATOR

Sixiao Huang, Southern University of Science and Technology, CN; Tintin Wang, Southern University of Science and Technology, CN; Ang Li, Southern University of Science and Technology, CN; Ao Shen, Southern University of Science and Technology, CN; Kai Li, Southern University of Science and Technology, CN; Keyao Jiang, Southern University of Science and Technology, CN; Mingqiang Huang, Southern University of Science and Technology, CN; Hao Yu, Southern University of Science and Technology, CN

AN INNOVATIVE MEMORY DESIGN WITH INTERNAL ECC FUNCTIONALITY BASED ON IN-MEMORY COMPUTING

Bai Na, Anhui University, CN; Li Gang, Anhui University, CN; Xu Yaohua, Anhui University, CN; Wang Yi, Anhui University, CN; Ming Tianbo, Anhui University, CN; Xu Yongjian, National University of Defense Technology, CN; Liu Biwei, National University of Defense Technology, CN

BLACK-BOX AUTO-TUNING FOR CUSTOMIZED SSD FIRMWARE PARAMETERS UNDER CONSTRAINTS

Kibeen Jung, Samsung, KR; Changyong Oh, Samsung, KR; Hyun-kyo Oh, Samsung, KR; Byeonghui Kim, Samsung, KR; Hankyu Lee, Samsung, KR; Seongho Roh, Samsung, KR; Youngjae Bae, Samsung, KR; Donghyub Kang, Samsung, KR; Sangkwon Moon, Samsung, KR; Kangho Roh, Samsung, KR; Jisoo Kim, Samsung, KR; Sangyeun Cho, Samsung, KR; Jongyoul Lee, Samsung, KR

CLEAR-HD: COMPUTATIONALLY LIGHT AND EFFECTIVE UNLEARNING FOR HYPERDIMENSIONAL COMPUTING

Fatemeh Asgarinejad, UCSD, US; Tajana Rosing, UCSD, US; Baris Aksanli, San Diego State University, US

COMPACT THERMAL MODEL-BASED ANALYTICAL 3D CHIP PLACEMENT WITH GPU ACCELERATION

Zijie Geng, University of Science and Technology of China, CN; Zhaojie Tu, University of Science and Technology of China, CN; Jie Wang, University of Science and Technology of China, CN; Yuxi Qian, University of Science and Technology of China, CN; Siyuan Xu, Huawei, CN; Mingxuan Yuan, Huawei, HK; Jianye Hao, Tianjin University, CN

COMPUTING-IN-MEMORY DATAFLOW FOR MINIMAL BUFFER TRAFFIC

Choongseok Song, Hanyang University, KR; Doo Seok Jeong, Hanyang University, KR

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

DAPO: DESIGN STRUCTURE AWARE PASS ORDERING IN HIGH-LEVEL SYNTHESIS WITH GRAPH CONTRASTIVE AND REINFORCEMENT LEARNING

Jinming Ge, Hong Kong University of Science and Technology (HKUST), HK; Linfeng Du, The Hong Kong University of Science and Technology, HK; Likith Anaparty, Indian Institute of Technology (IIT) Palakkad, IN; Shangkun Li, The Hong Kong University of Science and Technology, HK; Tingyuan Liang, The Hong Kong University of Science and Technology, HK; Afzal Ahmad, Hong Kong University of Science and Technology (HKUST), HK; Vivek Chaturvedi, Indian Institute of Technology (IIT) Palakkad, IN; Sharad Sinha, Indian Institute of Technology (IIT) Goa, IN; Zhiyao Xie, Hong Kong University of Science and Technology (HKUST), HK; Jiang Xu, Hong Kong University of Science and Technology (HKUST), Guangzhou, CN; Wei Zhang, Hong Kong University of Science and Technology (HKUST), HK

DEAD GATE ELIMINATION

Yanbin Chen, Technical University of Munich, DE; Helmut Seidl, Technical University of Munich, School of CIT, DE; Christian Mendl, Technical University of Munich, DE

DIRECTED ON-THE-FLY VALIDATION OF HIERARCHICAL CACHE COHERENCE PROTOCOLS

Abhinaba Chakraborty, imec, BE; Ansuman Banerjee, Indian Statistical Institute, IN; Vinay B.Y. Kumar, imec, BE; Arindam Mallik, imec, BE

EDGE CONTINUAL LEARNING WITH MIXED-SIGNAL GAUSSIAN MIXTURE-BASED BAYESIAN NEURAL NETWORKS

Steven Davis, University of Notre Dame, US; Zephan Enciso, University of Notre Dame, US; Likai Pei, University of Notre Dame, US; Jianbo Liu, University of Notre Dame, US; Boyang Cheng, University of Notre Dame, US; Danny Chen, University of Notre Dame, US; Ningyuan Cao, University of Notre Dame, US

EFFICIENT RUNTIME MANAGEMENT OF CROSSBARS FOR PATH-BASED IN-MEMORY COMPUTING

Sven Thijssen, Florida Atlantic University, US; Muhammad Rashedul Haq Rashed, University of Texas at Arlington, US; Sumit Jha, Florida International University, US; Rickard Ewetz, University of Florida, US

EVOSOLO: EVOLUTIONARY SEQUENCE OPTIMIZATION FOR LOGIC SYNTHESIS WITH CASCADED PPO

Jiaxing Wang, Huazhong University of Science and Technology, CN; Dan Feng, Huazhong University of Science and Technology, CN; Kang Liu, Huazhong University of Science and Technology, CN

FARM: FAST ACCELERATION OF RANDOM FORESTS VIA IN-MEMORY PROCESSING

Aymen Ahmed, University of Michigan, US; Valeria Bertacco, University of Michigan, US

FAXC: EXPLOITING FEATURE APPROXIMATION FOR PRIVACY PRESERVATION IN HUMAN ACTIVITY RECOGNITION

Nishanth Chennagouni, University of New Hampshire, US; Sandeep Sunkavilli, University of New Hampshire, US; Qiaoyan Yu, University of New Hampshire, US

FAST RANDOM WALK THROUGH REDUCTION OF ABSORBING MARKOV CHAIN

Wonjae Lee, KAIST, KR; Daijoon Hyun, Sejong University, KR; Youngsoo Shin, KAIST, KR

FUNCFORMER: CIRCUIT REPRESENTATION LEARNING VIA THE FLOW OF FUNCTIONAL PROPAGATION

Zhihai Wang, University of Science and Technology of China, CN; Yunjie Ji, University of Science & Technology of China, CN; Jie Wang, University of Science and Technology of China, CN; Min Li, Huawei, CN; Junhua Huang, Huawei, CN; Zhihao Shi, University of Science and Technology of China, CN; Mingxuan Yuan, Huawei, HK; Jianye Hao, Tianjin University, CN

GENESIS: A SPIKING NEUROMORPHIC ACCELERATOR WITH ON-CHIP CONTINUAL LEARNING

Vedant Karia, University of Texas at San Antonio, US; Abdullah Zyarah, University of Texas at San Antonio, US; Dhireesha Kudithipudi, University of Texas San Antonio, US

GTA: AN INSTRUCTION-DRIVEN GRAPH TENSOR ACCELERATOR FOR GENERAL GNNS

Kai Zhong, Tsinghua University, CN; Jin Si, University of Oxford, CN; Zhenhua Zhu, Tsinghua University, CN; Qiushi Lin, Tsinghua University, CN; Marc Neu, Karlsruhe Institute of Technology, DE; Juergen Becker, Karlsruhe Institute of Technology, DE; Huazhong Yang, Tsinghua University, CN; Yu Wang, Tsinghua University, CN

GUARD RING- AND DIFFUSION-SHARING EMBEDDED FINFET ARRAY PLACEMENT

Shih-Yu Chen, National Yang Ming Chiao Tung University, TW; Tzu-Hsiang Wei, National Yang Ming Chiao Tung University, TW; Hao-Ju Chang, National Yang Ming Chiao Tung University, TW; Hung-Ming Chen, Institute of Electronics, National Yang Ming Chiao Tung University, TW; Chien-Nan Liu, National Yang Ming Chiao Tung University, TW

HETEROGENEOUS APPROXIMATE MULTIPLICATIONS: A NEW FRONTIER FOR PRACTICAL DNNS

Salar Shakibhamedan, TU Wien, AT; Nima Amirafshar, Heidelberg University, DE; Axel Jantsch, TU Wien, AT; Nima TaheriNejad, Heidelberg University, DE

HLSRANKER: DESIGN SPACE EXPLORATION IN HIGH-LEVEL SYNTHESIS USING PREFERENCE BAYESIAN OPTIMIZATION

Renjing Hou, Beijing University of Posts and Telecommunications, CN; Donghao Guo, Beijing University of Posts and Telecommunications, CN; Zhe Lin, Sun Yat-sen University, CN; Peng Xu, The Chinese University of Hong Kong, HK; Jiawei Liu, Beijing University of Posts and Telecommunications, CN; Jianwang Zhai, Beijing University of Posts and Telecommunications, CN; Kang Zhao, Beijing University of Posts and Telecommunications, CN

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

INHERENT VULNERABILITY OF ATOMIC PATTERNS DUE TO DISTINGUISHABILITY OF FIELD MULTIPLICATION AND SQUARING OPERATIONS

Alkistis Sigourou, IHP GmbH - Leibniz Institute for High Performance Microelectronics, DE; Zoya Dyka, IHP GmbH - Leibniz Institute for High Performance Microelectronics, BTU Cottbus-Senftenberg, DE; Peter Langendoerfer, IHP GmbH - Leibniz Institute for High Performance Microelectronics, BTU Cottbus-Senftenberg, DE; Ievgen Kabin, IHP - Leibniz-Institute innovative Mikroelektronik, DE

LEDRO: LLM-ENHANCED DESIGN SPACE REDUCTION AND OPTIMIZATION FOR ANALOG CIRCUITS

Dimple Kochar, Massachusetts Institute of Technology, US; Hanrui Wang, Massachusetts Institute of Technology, US; Anantha Chandrakasan, Massachusetts Institute of Technology, US; Xin Zhang, IBM, US

LLM-DRIVEN TPU DESIGN: CRAFTING CUSTOM TENSOR PROCESSING ACCELERATORS WITH APTPU-GEN

Deepak Vungarala, New Jersey Institute of Technology, US; Mohammed E. Elbtity, University of South Carolina, US; Sumiya Syed, New Jersey Institute of Technology, US; Sakila Alam, New Jersey Institute of Technology, US; Kartik Pandit, New Jersey Institute of Technology, US; Arnob Ghosh, New Jersey Institute of Technology, US; Ramtin Zand, University of South Carolina, US; Shaahin Angizi, New Jersey Institute of Technology, US

LUT-MM: AN EFFICIENT LOOKUP TABLE-BASED APPROACH FOR MODULAR MULTIPLICATION

Zhaoyuan Li, Zhejiang University, CN; Kun Yang, Zhejiang University, CN; Kui Ren, Zhejiang University, CN

MACHINE LEARNING DRIVEN EARLY CLUSTERING FOR MULTI-BIT FLIP-FLOP ALLOCATION

Jooyeon Jeong, Seoul National University, KR; Taewhan Kim, Seoul National University, KR

METAGUARD: TRANSFORMING RUN-TIME HARDWARE TROJAN DETECTION USING META REINFORCEMENT LEARNING

Zhangying He, California State University, Long Beach, US; Thomas Nguyen, California State University, Long Beach, US; Hossein Sayadi, California State University, Long Beach, US

MODELING PFAS IN SEMICONDUCTOR MANUFACTURING TO QUANTIFY TRADE-OFFS IN ENERGY EFFICIENCY AND ENVIRONMENTAL IMPACT OF COMPUTING SYSTEMS

Mariam Elgamal, Harvard University, US; Abdulrahman Mahmoud, MBZUAI, United Arab Emirates; Gu-Yeon Wei, Harvard University, US; David Brooks, Harvard University, US; Gage Hills, Harvard University, US

NAVIGATING THE TRILEMMA: SECURITY, POWER, AND PERFORMANCE TRADE-OFFS IN BLUETOOTH LOW ENERGY

Ning Miao, University of California, Davis, US; Chongzhou Fang, University of California, Davis, US; Ruijie Fang, University of California, Davis, US; Ruoyu Zhang, University of California, Davis, US; Setareh Rafatirad, University of California Davis, US; Hossein Sayadi, California State University, Long Beach, US; Houman Homayoun, University of California Davis, US

NON-NEGATIVE ADDERNET (NNAN): CAN WE MAKE DNNS MORE SECURE AND EFFICIENT WITHOUT MULTIPLICATION?

Yunxiang Zhang, Binghamton University, US; Sabbir Ahmed, Binghamton University, US; Abeer Almalky, Binghamton University, US; Adnan Siraj Rakin, Binghamton University, US; Wenfeng Zhao, Binghamton University, US

ONE GRAY CODE FITS ALL: OPTIMIZING ACCESS TIME WITH BI-DIRECTIONAL PROGRAMMING FOR QLC SSDS

Tianyu Wang, Shenzhen University, CN; Shaoqi Li, Shenzhen University, CN; Yongbiao Zhu, Shenzhen University, CN; Fuwen Chen, Shenzhen University, CN; Chenlin Ma, Shenzhen University, CN; Zhaoyan Shen, Shandong University, CN; Rui Mao, Shenzhen University, CN; Yi Wang, Shenzhen University, CN

ORDERING-CENTRIC: A SCALABLE AND EXACT METHOD FOR SCHEDULING WITH RESOURCE CONSTRAINTS

Meng Gao, State Key Lab of Processors, Institute of Computing Technology, CAS, CN; Jiacheng Zhao, State Key Lab of Processors, Institute of Computing Technology, CAS, CN; Huimin Cui, State Key Lab of Processors, Institute of Computing Technology, CAS, CN; Xiaobing Feng, State Key Lab of Processors, Institute of Computing Technology, CAS, CN

OPTIMAL FRONT VS BACK-SIDE SIGNAL ALLOCATION FOR PPA IMPROVEMENTS IN ADVANCED CMOS FEATURING BACK-SIDE METAL INTERCONNECTS

Nishant Gupta, University of Texas at Austin, US; Sirish Oruganti, The University of Texas at Austin, US; Sai Subrahmanya Teja Nibhanupudi, The University of Texas at Austin, US; Anup Ashok Kedilaya, University of Texas At Austin, US; Xiuhao Zhang, The University of Texas at Austin, US; Jaydeep Kulkarni, University of Texas at Austin, US

OUT OF THE BOX TECHNIQUES FOR DATA PATH VERIFICATION

Atharva Kakde, Cadence Design Systems, Inc., IN; Ketki Gosavi, Cadence Design Systems, Inc., IN; Pradeep Bagavathiappan, Cadence Design Systems, Inc., IN; Anshul Singhal, Cadence Design Systems, Inc., IN

QUANTUM SECURE HASH ORACLE (QSHO): STRENGTHENING POST-QUANTUM CRYPTOGRAPHY WITH KYBER-AES, GROVER'S SIMULATIONS, AND HYBRID ATTACK RESISTANCE

Mohamed Yaqub, SRM Institute of Science and Technology, IN; Adarsh Anandhakumar, SRM Institute of Science and Technology, IN; Sudikshan Senthilkumaran, SRM Institute of Science and Technology, IN; Navin Balaji, SRM Institute of Science and Technology, IN; Gayathri Mani, SRM Institute of Science and Technology, IN; Pushpalatha M, SRM Institute of Science and Technology, IN

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

OPT-MC: A GRAPH-BASED PLACEMENT AND ROUTING ALGORITHM FOR OPTIMIZING MACRO CELL DESIGN

ByeongKeun Kang, Samsung, KR; YoonJung Kim, Samsung, KR; JungSeok Hwang, Samsung, KR; DooYoung Lee, Samsung, KR; MooKyu Bae, Samsung, KR; MinKwon On, Samsung, KR; HyunSeo Kang, Samsung, KR; JungSeok Oh, Samsung, KR; WanDong Kim, Samsung, KR; HyuckJoon Kwon, Samsung, KR; JiHo Cho, Samsung, KR; Ki-Whan Song, Samsung, KR; SungHoi Hur, Samsung, KR

PACEMAKER: ENERGY-EFFICIENT SPECULATIVE SCHEDULING WINDOW RESIZING WITHOUT PERFORMANCE IMPACT

Jeonghoon Choi, Yonsei University, KR; Ipoom Jeong, Yonsei University, KR; Won Woo Ro, Yonsei University, KR

PAGO: PARETO-ASSISTED GOAL OPTIMIZATION FOR ANALOG CIRCUIT SIZING

Youngchan Jo, Hanyang University, KR; Jaemyung Lim, Hanyang University, KR

PANTHER: A PIM-BASED BLOCKCHAIN DATABASE SYSTEM SUPPORTING EFFICIENT VERIFIABLE QUERIES

Yifan Hua, Shanghai Jiao Tong University, CN; Shengan Zheng, Shanghai Jiao Tong University, CN; Weihan Kong, Shanghai Jiao Tong University, CN; Yuheng Wen, Shanghai Jiao Tong University, CN; Linpeng Huang, Shanghai Jiao Tong University, CN

PARLS: A LOGIC SYNTHESIS FRAMEWORK BASED ON CIRCUIT PARTITIONING AND REINFORCEMENT LEARNING

Xingyu Qin, Beijing University of Posts and Telecommunications, CN; Guande Dong, Beijing University of Posts and Telecommunications, CN; Jianwang Zhai, Beijing University of Posts and Telecommunications, CN; Kang Zhao, Beijing University of Posts and Telecommunications, CN

PATHE: A PRIVACY-PRESERVING MASS SPECTROMETRY DATABASE PATTERN SEARCH PLATFORM WITH FULLY HOMOMORPHIC ENCRYPTION

Xuan Wang, University of California San Diego, US; Minxuan Zhou, Illinois Tech, US; Yujin Nam, UCSD, US; Gabrielle De Micheli, UC San Diego, US; Sumukh Pinge, University of California, San Diego, US; Augusto Vega, IBM Research, US; Tajana Rosing, UCSD, US

PIPESPEC: BREAKING STAGE DEPENDENCIES IN HIERARCHICAL LLM DECODING

Bradley McDanel, Franklin and Marshall College, US; Sai Qian Zhang, New York University, US; Yunhai Hu, New York University, US; Zining Liu, University of Pennsylvania, US

PI-WHISPER: DESIGNING AN ADAPTIVE AND INCREMENTAL AUTOMATIC SPEECH RECOGNITION SYSTEM FOR EDGE DEVICES

Amir Nassereldine, University at Buffalo, US; Dancheng Liu, SUNY Buffalo, US; Chenhui Xu, University at Buffalo, US; Ruiyang Qin, University of Notre Dame, US; Yiyu Shi, University of Notre Dame, US; Jinjun Xiong, University at Buffalo, US

PLACE-AND-ROUTE FOR PHOTONIC INTEGRATED CIRCUITS USING INDUSTRY-STANDARD EDA TOOLS

Georgios Kyriazidis, Harvard University, US; John Davis, Harvard University, US; Jui-Hung Chang, National Cheng Kung University, TW; Chih-Lung Lin, National Cheng Kung University, TW; Gage Hills, Harvard University, US

PMICO: POWER MANAGEMENT INTEGRATED CIRCUITS OPTIMIZATION FRAMEWORK USING MULTI-AGENT REINFORCEMENT LEARNING

Han Wu, Southern University of Science and Technology, CN; Haoqiang Deng, Southern University of Science and Technology, CN; Yan Lu, Tsinghua University, CN; Bo Yuan, Southern University of Science and Technology, CN; Junmin Jiang, Southern University of Science and Technology, CN

PPA-DRIVEN PLACEMENT VIA ADAPTIVE CLUSTER CONSTRAINTS OPTIMIZATION

Ziyan Liu, University of Science and Technology of China, CN; Siyuan Xu, Huawei, CN; Jie Wang, University of Science and Technology of China, CN; Zijie Geng, University of Science and Technology of China, CN; Yeqiu Chen, University of Science and Technology of China, CN; Mingxuan Yuan, Huawei, HK; Jianye HAO, Tianjin University, CN; Feng Wu, University of Science and Technology of China, CN

PROCESS DESIGN KITS FOR CO-DESIGNING BROADBAND INTEGRATED PHOTONICS AND SILICON CMOS IN ELECTRONIC-PHOTONIC VLSI CIRCUITS

Georgios Kyriazidis, Harvard University, US; John Davis, Harvard University, US; Jui-Hung Chang, National Cheng Kung University, TW; Hana Warner, Harvard University, US; Norman Lippok, Wellman Ctr. for Photomedicine, US; Chih-Lung Lin, National Cheng Kung University, TW; Benjamin Vakoc, Wellman Ctr. for Photomedicine, US; Marko Loncar, Harvard University, US; Gage Hills, Harvard University, US

PROMPTV: LEVERAGING LLM-POWERED MULTI-AGENT PROMPTING FOR HIGH-QUALITY VERILOG GENERATION

Zhendong Mi, Stevens Institute of Technology, US; Renming Zheng, Xi'an Jiaotong-Liverpool University, CN; Haowen Zhong, University of Washington, US; Yue Sun, LEHIGH UNIVERSITY, US; Shaoyi Huang, Stevens Institute of Technology, US

RAINY NOISE CANCELLATION TECHNIQUE FOR LIDAR SYSTEM USING CONVOLUTION NEURAL NETWORK

ching-hwa cheng, Feng-Chia University, TW

RETHINKING THE DISTRIBUTION OF OUTLIERS IN LARGE LANGUAGE MODELS: AN IN-DEPTH STUDY

Rahul Raman, NYU, US; Khushi Sharma, New York University, US; Sai Qian Zhang, New York University, US

RETHINKING TRANSLATION ROBUSTNESS FOR RELIABLE CONVOLUTIONAL SEGMENTATION ARCHITECTURE

Zherui Zhang, Beijing University of Posts and Telecommunications, CN

MONDAY WORK-IN-PROGRESS POSTER RECEPTION (continued)

ROPE-MLA: ROW-ACCESS OPTIMIZED PROCESSING ELEMENT MACHINE LEARNING ACCELERATOR

Prasanth Prabu Ravichandiran, North Carolina State University and Nvidia, US; Paul Franzon, NCSU, US; W. Rhett Davis, North Carolina State University, US; Tianfu Wu, North Carolina State University, US; Franc Brglez, NC State University, US

RTLEXPLAIN: A STRUCTURED APPROACH TO RTL CODE SUMMARIZATION AND QUESTION ANSWERING FOR MEDIUM-TO-LARGE DESIGNS USING LLMS

Ting-Hsun Chi, National Taiwan University, TW; Charles Mackin, IBM Research, US; Luyao Shi, IBM Research, US; Prashanth Vijayaraghavan, IBM Research, US; Hsinyu Tsai, IBM, US; Ehsan Degan, IBM, US

SCALEX: A SCALABLE AND FLEXIBLE ARCHITECTURE FOR EFFICIENT GNN INFERENCE

Tingting Xiang, National University of Singapore, SG; Miao Yu, National University of Singapore, SG; Trevor E. Carlson, National University of Singapore, SG

SELF-SUPERVISED LEARNING BASED ETCHING PROCESS MODELING: BRIDGING SIMULATION AND EXPERIMENTAL DATA

Zhenjie Yao, IMECAS, CN; Ziyi Hu, IMECAS, CN; Zhiqiang Li, IMECAS, CN; Dashan Shang, Institute of Microelectronics, Chinese Academy of Sciences, CN; Rui Chen, IMECAS, CN; Ling Li, IMECAS, CN

SLTARCH: TOWARDS SCALABLE POINT-BASED NEURAL RENDERING BY TAMING WORKLOAD IMBALANCE AND MEMORY IRREGULARITY

Xingyang Li, Shanghai Jiao Tong University, CN; Jie Jiang, Shanghai Jiao Tong University, CN; Yu Feng, Shanghai Jiao Tong University, CN; Yiming Gan, Institute of Computing Technologies, Chinese Academy of Sciences, CN; Jieru Zhao, Shanghai Jiao Tong University, CN; Zihan Liu, Shanghai Jiao Tong University, CN; Jingwen Leng, Shanghai Jiao Tong University, CN; Minyi Guo, Shanghai Jiao Tong University, CN

SYSTEMVERILOG ASSERTION SYNTAX CORRECTION WITH KNOWLEDGE DISTILLATION: TOWARD LLM-GUIDED AUTOMATED HARDWARE VERIFICATION

Dipayan Saha, University of Florida, US; Chandra Bhagavatula, ChipStack, Inc., US; Ryan Eiger, ChipStack, Inc., US; Kartik Hedge, ChipStack, Inc., US; Hamid Shojaei, ChipStack, Inc., US; Farimah Farahmandi, University of Florida, US

SYNTHESIS OF A MEMRISTOR-TRANSISTOR SINGLE-PHASE CELL LIBRARY AND ITS USE TO SYNTHESIZE LOGIC CIRCUITS

Baishakhi Rani Biswas, University of Southern California, US; Sandeep Gupta, University of Southern California, US

TOWARDS ACCURATE, REAL-TIME, AND ENERGY-EFFICIENT ATTENTION MONITORING

Anice Jahanjoo, TU Wien, AT; Vimala Bauer, Heidelberg University, DE; Soheil Khooyooz, Heidelberg University, DE; Mostafa Haghi, Heidelberg University, DE; Nima TaheriNejad, Heidelberg University, DE

TOWARDS MULTI-OBJECTIVE ROUTING: A NOVEL CORESET-BASED TRANSFER LEARNING FRAMEWORK

Xianglu Wang, University of Science and Technology of China, CN; Hu Ding, University of Science and Technology of China, CN

TRANSISTOR PLACEMENT ROUTABILITY PREDICTION FOR STANDARD CELL DESIGN

Vitor Hugo Fuerstenau, UFRGS, BR; Felipe Bortolon, Silvaco, BR; Marcos Backes, Silvaco, BR; Eduardo Barbian, Silvaco, BR; Ricardo Reis, UFRGS, BR

TRUSTCHAIN AI: A PRIVACY-PRESERVING DECENTRALIZED ARCHITECTURE FOR LARGE LANGUAGE MODEL AGGREGATION

Arpita Sarker, Ms, DE; Alexander Jesser, Prof. Dr., DE

VALIDATING THE DESIGN OF CPS: INTERFACING SIMULATIONS OF MULTI-PHYSICS COMPONENTS AND SOFTWARE WITH CONTRACT-BASED MONITORING

Friederike Bruns, University of Oldenburg, DE; Francesco Tosoni, University of Verona, IT; Sven Mehlhop, OFFIS e.V., DE; Andreas Rauh, Carl von Ossietzky Universität, DE; Sara Vinco, Politecnico di Torino, IT; Jörg Walter, OFFIS e.V., DE; Frank Oppenheimer, OFFIS e.V., DE; Franco Fummi, University of Verona, IT

POG: PARAMETER OPTIMIZATION USING GRAPH NEURAL NETWORKS ON REINFORCEMENT LEARNING

Sumin Oh, Hyunjin Kim, Dankook University, KR

ENABLING THE AI REVOLUTION

Time: 8:45 AM - 10:00 AM

Session Type: Keynote

Topic Area(s): EDA

Room: 3007, Level 3

Description: The hype surrounding AI has reached unprecedented levels, with governments and industries engaged in an arm's race towards Artificial General Intelligence. As AI permeates every aspect of our lives, from smart sensors and hearing aids to automotive, robotics, and high-energy particle physics, we face a diverse range of challenges that extend far beyond the widely discussed performance scalability and sustainability.

These challenges include demanding requirements such as nanosecond latency, tiny footprints, functional safety, and a high degree of customization.

This talk provides insights into the broad emerging spectrum of AI applications and discusses our latest research demonstrating how these challenges, ranging from bag tagging to 6G, can be addressed through silicon diversity, agile AI stacks and innovative solutions.

Speaker: Michaela Blott, Advanced Micro Devices (AMD)

IEEE 2416 SYSTEM POWER MODELING WORKING GROUP OPEN MEETING: SPONSORED BY SI2

Time: 10:00 AM - 11:30 AM

Session Type: Additional Meeting

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: In the current dynamically changing landscape of computing, growth of artificial intelligence (AI) applications have caused an exponential increase in energy consumption, re-emphasizing the need for managing power footprint in chip design. To manage this escalating energy footprint and enabling true system level low power design, modeling standards play a key role to facilitate inter-operability and re-use. IEEE 2416, the "IEEE Standard for Power Modeling to Enable System Level Analysis", introduced in 2019, offers a unified framework spanning system-level to detailed design, facilitating comprehensive low power design for entire systems. This standard also enables efficiency through contributor-based Process, Voltage, and Temperature (PVT) independent power modeling.

IEEE 2416-2025 will include production industry-driven extensions in analog/mixed-signal, system modeling, and multi-voltage scenarios. Join this open meeting of the IEEE 2416 Working Group to learn how the upcoming release will enhance system power modeling productivity for you and your company. Attendees will include system designers and architects, logic and circuit designers, validation engineers, CAD managers, researchers, and academicians.

Speaker: Nagu Dhanwada, IBM, US; Leigh Anne Clevenger, Si2, Inc., US

VIEW FROM WALL STREET

Time: 10:15 AM - 11:00 AM

Topic Area(s): EDA

Session Type: Analyst Presentation

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: We will examine the financial performance and key business metrics of the EDA industry through 2024, the further consolidation of EDA (the combination of Synopsys-Ansys), as well as the material technical and market trends and requirements that have influenced EDA business performance and strategies. Among the trends, we will again examine the progression of semiconductor R&D spending and how the market values of the publicly-held EDA companies have evolved. Lastly, we will provide our updated financial projections for the EDA industry for 2025 and 2026.

Speaker: Jay Vleeschhouwer, Griffin Securities, US

INTELLIGENT EXTRACTION OF ADVANCED IC PACKAGE

Time: 10:30 AM - 11:00 AM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The need for modern workloads in the latest innovations has brought 2.5D/3D stacking and advanced packaging technologies to the forefront. The requirements for integrating multiple chips, components, and materials to create an advanced IC package are becoming increasingly complicated and introduce new challenges to existing extraction and analysis methods. A computational framework which allows for comprehensive extraction of advanced IC package designs is proposed. It is based on a hybrid computational framework, combining different electromagnetic (EM) solvers, and leveraging AI models based on 3D full-wave simulation, to extract different netlist models efficiently and accurately for system-level analysis and optimization. It has the capability to do entire extraction of the most intricate stacked die system for a variety of packaging styles and provides co-design automation flows with signoff extraction, static timing analysis (STA) and signoff with signal and power integrity (SI/PI). With exceptional performance and reliability, it enables users to meet tight schedule efficiently.

Speaker: Xiaoyan Xiong, Yingxin Sun, Cadence Design Systems, Inc., US; Jiyue Zhu, Gang Kang; Jian Liu, Cadence Design Systems, Inc.

AI-ENABLED EDA FOR CHIP DESIGN

Time: 10:30 AM - 12:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2008, Level 2

Description: Artificial Intelligence is revolutionizing Electronic Design Automation (EDA), accelerating innovation in chip design and verification. This panel brings together four technical experts - each a co-founder of their company - who are pioneering AI-driven solutions to tackle today's most complex semiconductor challenges. From automating circuit optimization to enhancing verification efficiency, our panelists will showcase cutting-edge tools that push the boundaries of performance, accuracy, and scalability. Attendees will gain deep technical insights into real-world AI applications in EDA, uncovering how machine learning is reshaping the design flow and redefining engineering productivity. Whether you're a design engineer, verification specialist, or EDA technology strategist, this discussion will provide valuable perspectives on the future of AI in semiconductor design.

Organizer(s): Predrag Nikolic, Veriest Solutions Ltd., RS

Moderator: Predrag Nikolic, Veriest Solutions Ltd., RS

Speakers: Kartik Hegde, ChipStack, Inc., US; Aakash Levy, Silimate, Inc., US; Badru Agarwala, Rise Design Automation, Inc., US; William Wang, ChipAgents.ai, US; Sandeep Srinivasan, VerifAI; Jeffrey Pan, Bronco AI; Madhulima Tewari, Verifaix

FROM DEVICES TO DEBUG - MODELING THOUGHTFUL DESIGN PRACTICES

Time: 10:30 AM - 12:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2012, Level 2

Description: Learn from the smorgasboard skillset needed to dive deep into the world of devices to working devices that deliver impactful semiconductors cost effectively - from transistor devices, PDK and models to debugging parts and interconnect design.

- **Machine Learning (ML) Assisted IBIS-AMI Model for Optical Module Involved Advanced SerDes System Designs**
  Ruoshi Xu, Zeqin Lu, Xinying Wang, Curtis Clark, Saeed Asgari, Wei-hsing Huang, Bozidar Novakovic, Dylan McGuire, Ansys, CA
- **Recalibration of MOSFET Compact Models based on Complex Product-Related Layouts using Bayesian Optimization**
  Lan Luo, David Winston, Robert Perricone, Bria Matthews, Richard Wachnik, IBM, US
- **Enhancing PDK Library Validation with Machine Learning. A Novel Approach to Layout Comparison**
  Nolan Pavek, Romain Feuillette, Farzana Akhter, GlobalFoundries, US
- **A Novel Structure to Achieve Broadcastable IJTAG Network**
  Feilong Pan, Minqiang Peng, Lei Yang, Keqing Ouyang, Guohua Zhou, Sanechips Technology Co.,Ltd, CN
- **Generation of Failure Inspection Pattern without Design Impact during P&R in BSPDN Design**
  Woojin Jin, Sangun Park, Joowan Lee, Haemin Yoo, TaeYang You, Samsung, KR
- **MCP Induced Glitches**
  Dinesh Joshi; Nidhi Sinha

Session Chair(s): Lakshmanan Balasubramanian, Texas Instruments

WATT'S NEXT: LOW-POWER DESIGN AND VERIFICATION TRENDS

Time: 10:30 AM - 12:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2010, Level 2

Description: Accurate power analysis is crucial for designing power-optimized silicon, especially as modern applications demand higher performance within stringent power and thermal constraints. In this session, presenters will share their experiences and insights into advanced power analysis techniques and optimization strategies across a wide range of applications.

- **Streamlining Low Power Verification for Multi-die SoCs: A Comprehensive Framework**
  Jaein Hong, Junha Jeon, Yujin Oh, Moonki Jun, Sanghune Park, Samsung, KR
- **UPF Guided Design Editing for Early Low Power Verification Sign Off**
  Ankit Narang, Sachin Bansal, Vishal Keswani, M.Vaishnavi Reddy, Amit Goldie, Manish Goel, Synopsys, IN
- **Enhancing RTL Power Accuracy with Advanced Buffer Modeling for Improved Efficiency and Correlation**
  Fengyu Xiao, Shixuan Que, Sai Li, Lei Bao, Ling Sun, Iluvatar, CN; Zhongming Hou, Zhenbang Wang, Ansys, CN
- **Unveiling the Core Truth: Advanced Glitch Power Analysis and Optimization Using Statistical Methodology**
  Chenyang Zhang, Chen Lin, Jinbo Zhu, Yuchao Liu, Chao Gu, Sanechips Technology Co.,Ltd, CN; Zhongming Hou, Ansys, CN

- **A Novel Approach for Workload Based GPU Datapath Power Optimization**
  Deepayan Dasgupta, Tanuj Sengupta, Samsung, US
- **Optimal Power Estimation Methodology for CXL Memory Controllers**
  Kyeongseob Kim, SK hynix, KR

Session Chair(s): Chandrakanth Betageri, Intel Corporation

ADVENTURES IN PCBS, PARTITIONING, AND LEGALIZATION!

Time: 10:30 AM - 12:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: Buckle up for an adventure through the realms of PCBs, partitioning, and legalization! Start by exploring novel algorithms for PCB global placement and legalization. Next, dive into a GNN-based graph partitioning algorithm, followed by a fast deterministic parallel hypergraph partitioner. Then, explore multi-height cell legalization with TSMC's recent FinFlex standard cells that allows for better PPA. End your journey with a detailed placer that optimizes secondary power delivery network for multi-power domain designs.

- **Clearance-Constrained PCB Global Placement with Heterogeneous Components**
  Yan-Jen Chen, Wei-Kai Huang, Chung-Ting Tsai, Chiao-Yu Ou, Yao-Wen Chang, National Taiwan University, TW
- **Constraint Graph-based PCB Legalization Considering Dense, Heterogeneous, Irregular-Shaped, and Any-Oriented Components**
  Chiao-Yu Ou, Yan-Jen Chen, Yao-Wen Chang, National Taiwan University, TW
- **GPart: A GNN-Enabled Multilevel Graph Partitioner**
  Magi Chen, Ting-Chi Wang, National Tsing Hua University, TW
- **BlasPart: A Deterministic Parallel Partitioner for Balanced Large-Scale Hypergraph Partitioning**
  Shengbo Tong, Chunyan Pei, Wenjian Yu, Tsinghua University, CN
- **MIA-aware FinFlex Cell Legalization with Power-Driven Cell Version Substitution**
  Da-Wei Huang, Shao-Yun Fang, National Taiwan University of Science and Technology, TW
- **Secondary-Power-Cell-Aware Detailed Placement in Multiple Power Domain Designs**
  Yu-Wei Chang, Shao-Yun Fang, National Taiwan University of Science and Technology, TW; Kai-Chuan Yang, Min-Ching Lin, Synopsys, TW

Session Chair(s): Ankur Prasad, Apple Inc.; Yu-Guang Chen, National Central University, TW

AI ON FIRE: COMPUTE-IN-MEMORY AND MULTIPLICATION-FREE ACCELERATION FOR THE NEXT ERA

Time: 10:30 AM - 12:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3003, Level 3

Description: AI hardware is at an inflection point, demanding radical efficiency and performance leaps. This session dives into groundbreaking compute-in-memory (CIM) architectures, multiplication-free acceleration, and novel arithmetic paradigms that slash power and latency while boosting throughput. From LUT-based DNN accelerators to hybrid analog-digital computing and STT-MRAM-powered CIM, these innovations are setting AI hardware ablaze with new possibilities.

- **High Energy-efficiency and Low latency In-Memory Computing using Analog Accumulator and In-Memory ADC with shared References**
  Junyi Yang, Shuai Dong, Zhengnan Fu, Hongyang Shang, Arindam Basu, City University of Hong Kong, HK
- **CREST-CiM: Cross-Coupling-Enhanced Differential STT-MRAM for Robust Computing-in-Memory in Binary Neural Networks**
  Imtiaz Ahmed, Akul Malhotra, Sumeet Gupta, Purdue University, US
- **YOCO: A Hybrid In-Memory Computing Architecture with 8-bit Sub-PetaOps/W In-Situ Multiply Arithmetic for Large-Scale AI**
  Zihao Xuan, Wei Xuan, The Hong Kong University of Science and Technology, CN; Yuxuan Yang, Zijia Su, Song Chen, Yi Kang, University of Science and Technology of China, CN
- **ReSMiPS: A ReRAM-based Sparse Mixed-precision Solver with Fast Matrix Reordering Algorithm**
  Yuyang Fu, Jiancong Li, Zhiwei Zhou, Houji Zhou, Wenlong PengYi Li, Xiangshui Miao, Huazhong University of Science and Technology, CN; Jia Chen, The Hong Kong University of Science and Technology, HK
- **Lookup Table-based Multiplication-free All-digital DNN Accelerator Featuring Self-Synchronous Pipeline Accumulation**
  Hiroto Tagata, Takashi Sato, Hiromitsu Awano, Kyoto University, JP
- **WISEDRAM: A Reliable Bitwise In-DRAM Accelerator**
  Mohammad Arman Soleimani, Hamid Sarbazi-Azad, Sharif University of Technology, Iran; Nezam Rohbani, Institute for Research in Fundamental Sciences (IPM), Iran; Adrian Cristal Kestelman, Osman Unsal, Barcelona Supercomputing Center, ES

Session Chair(s): Ibrahim (Abe) Elfadel, IBM/ Khalifa University; Akhilesh Jaiswal, University of Wisconsin, Madison

AI UNDER ATTACK: ENHANCING PRIVACY, ROBUSTNESS, AND TRUST IN ML SYSTEMS

Time: 10:30 AM - 12:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3006, Level 3

Description: With the rapid evolution of AI technologies, ensuring robust security measures is crucial to mitigating risks and safeguarding sensitive data. This session explores cutting-edge research in AI security and privacy, addressing emerging threats and novel defenses across various machine learning paradigms. Topics include resilient federated learning on embedded devices, concealed backdoor attacks using machine unlearning, and continual novelty detection for intrusion detection systems. The session also covers secure inference of graph neural networks, privacy-preserving collaborative learning, and advancements in data-free knowledge distillation.

- **Resilient Federated Learning on Embedded Devices with Constrained Network Connectivity**
  Zihan Li, Han Liu, Ao Li, Ching-hsiang Chan, Yevgeniy Vorobeychik, William Yeoh, Ning Zhang, Washington University in St. Louis, US; Wenjing Lou, Virginia Polytechnic Institute and State University, US
- **ReVeil: Unconstrained Concealed Backdoor Attack on Deep Neural Networks using Machine Unlearning**
  Manaar Alam, Hithem Lamri, Michail Maniatakos, New York University, Abu Dhabi, AE
- **CND-IDS: Continual Novelty Detection for Intrusion Detection Systems**
  Sean Fuhrman, Onat Gungor, Tajana Rosing, University of California, San Diego, US
- **Graph in the Vault: Protecting Edge GNN Inference with Trusted Execution Environment**
  Ruyi Ding, Tianhong Xu, Aidong Adam Ding, Yunsi Fei, Northeastern University, US
- **Ensembler: Protect Collaborative Inference Privacy from Model Inversion Attack via Selective Ensemble**
  Dancheng Liu, SUNY Buffalo, US; Chenhui Xu, Jiajie Li, Amir Nassereldine, Jinjun Xiong, University at Buffalo, US
- **CAE-DFKD: Bridging the Transferability Gap in Data-Free Knowledge Distillation**
  Zherui Zhang, Wenhao Xu, Shibiao Xu, Jie Zhou, Li Guo, Beijing University of Posts and Telecommunications, CN; Changwei Wang, Qilu University of Technology, CN; Rongtao Xu, Institute of Automation, Chinese Academy of Sciences, CN; Yu Zhang, Tongji University, CN

Session Chair(s): Adnan Siraj Rakin, Binghamton University; Ayesha Siddique, University of Maine

BREAKING & SECURING THE FUTURE: ADVANCES IN SYSTEM & HARDWARE SECURITY

Time: 10:30 AM - 12:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3008, Level 3

Description: As cyber threats evolve and hardware vulnerabilities emerge, pioneering solutions are reshaping the landscape of security. Join this session for a deep dive into groundbreaking research at the crossroads of system security and hardware resilience. This session explores cutting-edge research at the intersection of system security and hardware resilience. We will examine novel defenses against control flow attacks on Intel SGX and AMD SEV, optimized data packing for homomorphic encryption to accelerate secure computation, and the discovery of a covert timing channel in cloud FPGAs. Additionally, we will uncover advanced fuzzing techniques for IoT protocol security, reverse engineering methods for extracting intelligence from vehicular CAN bus traffic, and a high-performance approach to control flow attestation in commodity MCUs. Attendees will gain insights into both emerging threats and innovative countermeasures shaping the future of secure computing.

- **On Bit-level Reverse Engineering of Vehicular CAN Bus**
  Yunlang Cai, Hanxue Shi, Xiaohang Wang, Haoting Shen, Li Lu, Kui Ren, Zhejiang University, CN
- **HoBBy: Hardening Unbalanced Branches against Control Flow Attacks on Intel SGX and AMD SEV**
  Chang Liu, Dongsheng Wang, Tsinghua University, CN; Shuaihu Feng, Yuan Li, Zhongguancun Laboratory, CN; Trevor Carlson, National University of Singapore, SG
- **CMFuzz: Parallel Fuzzing of IoT Protocols by Configuration Model Identification and Scheduling**
  Qi Xu, Fuchen Ma, Yuanliang Chen, Feifan Wu, Yanyang Zhao, Yu Jiang, Tsinghua University, CN; Wanli Chen, Heyuan Shi, Central South University, CN
- **A Novel Covert Timing Channel for Cloud FPGAs**
  Brian Udugama, CSIRO, AU; Darshana Jayasinghe, University of Sydney, AU; Hassaan Saadat, Aleksandar Ignjatovic, Sri Parameswaran, The University of Sydney, AU
- **RAP-Track: Efficient Control Flow Attestation via Parallel Tracking in Commodity MCUs**
  Antonio Joia Neto, Adam Caulfield, Ivan De Oliveira Nunes, Rochester Institute of Technology, US
- **An Enhanced Data Packing Method for General Matrix Multiplication in Brakerski/Fan-Vercauteren Scheme**
  Xiangchen Meng, Yan Tan, Zijun Jiang, Yangdi Lyu, Hong Kong University of Science and Technology, Guangzhou, CN

Session Chair(s): Hang Lu, Institute of Computing Technology, Chinese Academy of Sciences; Fengwei Zhang, Southern University of Science and Technology, SUSTech

NAVIGATING THE FRONTIERS OF NEURAL NETWORKS

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session features six papers of innovative research papers focused on advancing the efficiency and performance

- **An End-to-End FPGA Framework with Scalable Dataflow Architecture for Neuro-Symbolic AI**
  Hanchen Yang, Zishen Wan, Ritik Raj, Student, US; Joongun Park, Ziwei Li, Ananda Samajdar, Arijit Raychowdhury, Tushar Krishna, Georgia Institute of Technology, US
- **BitPattern: Enabling Efficient Bit-Serial Acceleration of Deep Neural Networks through Bit-Pattern Pruning**
  Gang Wang, Siqi Cai, Zhenyu Li, Wenjie Li, Dongxu Lyu, Yanan Sun, Jianfei Jiang, Guanghui He, Shanghai Jiao Tong University, CN
- **BLOOM: Bit-Slice Framework for DNN Acceleration with Mixed-Precision**
  Fangxin Liu, Ning Yang, Zongwu Wang, Shanghai Jiao Tong University, CN
- **ESM: A Framework for Building Effective Surrogate Models for Hardware-Aware Neural Architecture Search**
  Azaz-ur-Rehman Nasir, Samroz Ahmad Shoaib, Muhammad Abdullah Hanif, Muhammad Shafique, New York University, Abu Dhabi, AE
- **SnapPix: Efficient-Coding--Inspired In-Sensor Compression for Edge Vision**
  Weikai Lin, Yuhao Zhu, University of Rochester, US; Tianrui Ma, Institute of Computing Technology, Chinese Academy of Sciences, CN; Adith Boloor, Washington University, St. Louis, US; Yu Feng, Shanghai Jiao Tong University, CN; Ruofan Xing, Xuan Zhang, Northeastern University, US
- **Introducing Instruction-Accurate Simulators for Performance Estimation of Autotuning Workloads**
  Rebecca Pelke, Nils Bosbach, Lennart Reimann, Rainer Leupers, RWTH Aachen University, DE

Session Chair(s): Kai-Yuan (Kevin) Chao, Siemens; Amin Firoozshahian, Rain AI

SMARTER SYSTEMS: THE FUTURE OF HARDWARE EFFICIENCY IN AI

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: This session focuses on improving the efficiency of memory and hardware in machine learning systems. Papers presented here cover methods for optimizing hardware components and memory usage, as well as innovative strategies for applying quantization and pruning techniques to neural networks and recommendation systems, to reduce computational costs and power consumption.

- **Speculative Decoding for Verilog: Speed and Quality, All in One**
  Changran Xu, Yi Liu, Yunhao Zhou, Qiang Xu, The Chinese University of Hong Kong, HK; Shan Huang, Ningyi Xu, Shanghai Jiao Tong University, CN
- **PARO: Hardware-software Co-design with Pattern-aware Reorder-based Attention Quantization in Video Generation Models**
  Xinhao Yang, Tianchen Zhao, Hongyi Wang, Wenheng Ma, Shulin Zeng, Zhenhua Zhu, Xuefei Ning, Huazhong Yang, Yu Wang, Tsinghua University, CN
- **Hybrid Embedding Framework for Memory-Efficient Recommendation Systems**
  Seungjin Yang, Hyuk-Jae Lee, Seoul National University, KR; Chae Eun Rhee, Hanyang University, KR
- **Mixed-Precision Quantization for Deep Vision Models with Integer Quadratic Programming**
  Zihao Deng, Michael Orshansky, The University of Texas at Austin, US; Sayeh Sharify, Xin Wang, d-Matrix Corp., US
- **Maximizing Energy Efficiency in Spiking Neural Networks: A Dynamic Joint Pruning Framework**
  Shuo Chen, Zeshi Liu, Haihang You, Institute of Computing Technology, Chinese Academy of Sciences; Zhongguancun Laboratory, CN
- **DCDiff: : Enhancing JPEG Compression via Diffusion-based DC Coefficients Estimation**
  Ziyuan Zhang, Han Qiu, Chao Zhang, Tsinghua University, CN; Tianwei Zhang, Nanyang Technological University, SG; Bin Chen, Harbin Institute of Technology, CN

Session Chair(s): Chenhui Deng, NVIDIA; Liu Cheng, Institute of Computing Technology, Chinese Academy of Sciences, CN

SPIKE IT, SEE IT, SAY IT: NEXT-GEN AI PROCESSING

Time: 10:30 AM - 12:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: This section explores how next-generation hardware architectures are breaking the memory wall to accelerate large language models, computer vision, and neuromorphic computing for emerging AI systems. The first paper proposes a neuromorphic (spike-based) processor, which leverages spike-tracing bipolar-integrate-and-fire neurons. The second paper proposes an integrated image sensing and near-sensor MRAM-based processing architecture. The last four papers present cutting-edge research contributions addressing algorithm-hardware co-design for vision transformers (ViTs) and large language models (LLMs) on edge devices, pushing the boundaries of edge AI, offering new directions for efficient deployment of vision and language models in resource-constrained environments.

- **BiNeuroRAM: Energy-Efficient ReRAM-Based PIM for Accurate Bipolar Spiking Neural Network Acceleration**
  Jun Yan Lee, Chen Nie, Kang You, Yueyang Jia, Rui Yang, Zhezhi He, Shanghai Jiao Tong University, CN
- **ResISC: Residue Number System-Based Integrated Sensing and Computing for Efficient Edge AI**
  Sepehr Tabrizchi, Samin Sohrabi, Arman Roohi, University of Illinois, Chicago, US; MohammadReza Mohammadi, Ramtin Zand, University of South Carolina, US; Shaahin Angizi, New Jersey Institute of Technology, US
- **Efficient Edge Vision Transformer Accelerator with Decoupled Chunk Attention and Hybrid Computing-In-Memory**
  Yi Li, Zijian Ye, Songqi Wang, Ning Lin, Xiaojuan Qi, Han Wang, The University of Hong Kong, HK; Xiangqu Fu, Dashan Shang, Jinshan Yue, Feng Zhang, Institute of Microelectronics of the Chinese Academy of Sciences, CN; Shucheng Du, Beijing Institute of Technology, CN; Zhongrui Wang, Southern University of Science and Technology, CN
- **3D-CIMlet: A Chiplet Co-Design Framework for Heterogeneous In-Memory Acceleration of Edge LLM Inference and Continual Learning**
  Shuting Du, Luqi Zheng, Aradhana Mohan Parvathy, Feifan Xie, Tiwei Wei, Anand Raghunathan, Haitong Li, Purdue University, US
- **BlockPIM: Optimizing Memory Management for PIM-enabled Long-Context LLM Inference**
  Zhichun Li, Jun Zhou, Xueqi Li, Ninghui Sun, Institute of Computing Technology, Chinese Academy of Sciences, CN
- **PIMPAL: Accelerating LLM Inference on Edge Devices via In-DRAM Arithmetic Lookup**
  Yoonho Jang, Hyeongjun Cho, Yesin Ryu, Jungrae Kim, Seokin Hong, Sungkyunkwan University, KR

Session Chair(s): Xueqing Li, Tsinghua University; Wantong Li, University of California, Riverside

BEYOND LIMITS: PACKAGING, CRYOGENIC, AND NEW COOLING STRATEGIES FOR FUTURE COMPUTING

Time: 10:30 AM - 12:00 PM

Topic Area(s): Systems

Session Type: Research Panel

Room: 3012, Level 3

Description: As computing systems push toward ever-increasing performance, thermal management becomes a fundamental bottleneck. Cooling is no longer just a support function—it is a necessity to ensure that modern and future computing architectures achieve their full potential. The question remains: what is the best approach to keep computing efficient while overcoming thermal constraints? Should we rely on conventional package-level cooling, embed advanced and exotic cooling solutions within the 3D stack itself, or shift our focus toward developing thermally resilient devices that can operate at much higher temperatures? This panel will explore these three primary thermal management strategies. We will bring together experts from semiconductor manufacturing, system architecture, and thermal engineering to debate the merits, feasibility, and trade-offs of each approach. While cryogenic cooling remains an interesting avenue, the discussion will focus on the dominant and most practical cooling methods that can be broadly applied to computing systems today.

Organizer(s): Subhahish Mitra, Stanford University, US

Moderator: Mohamed Sabry Aly, NTU, SIngapore; Prof. David Atienza, ESL/EPFL, Switzerland

Speakers: John Wilson, Nvidia, US; Mircea Stan, University of Virginia, US; Jamil Kawa, Independent, US; Srabanti Chowdhury, Stanford University, US; Albert Zeng, Cadence Design Systems, Inc., US

AAA: ADVANCED AI ACCELERATORS

Time: 10:30 AM - 12:00 PM

Topic Area(s): AI

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: The rapid evolution of artificial intelligence (AI) has spurred unprecedented advancements in hardware accelerators, driven by the unique demands on computation and data movement of evolving AI models. This special session will spotlight cutting-edge AI accelerators developed by industry, highlighting innovative architectures and performance optimization techniques that are redefining scalability, energy efficiency, and processing speed in AI applications. The current status of AI accelerators, research direction in the field, and recommendations will be discussed. Attendees will gain insights on state-of-the-art hardware solutions for AI and real-world applications of these accelerators across domains such as cloud computing and edge devices.

- **Energy-Efficient On-Device AI Acceleration and More Enabled By 3D Integration**
  Tony Wu, Meta, US
- **Architecture and Design Approaches towards Large-scale AI Hardware Acceleration**
  Ashish Ranjan, IBM, US
- **SambaNova SN40L: Unleashing Agentic AI with Dataflow**
  Raghu Prabhakar, SambaNova Systems Inc, US

Organizer(s): Mingu Kang, University of California, San Diego, US; Jae-sun Seo, Cornell University, US

EDA IN THE CLOUD: OPTIMIZING CHIP DESIGN WORKFLOWS WITH GOOGLE CLOUD PLATFORM

Time: 11:15 AM - 11:45 AM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The electronic design automation (EDA) industry is evolving rapidly, and cloud computing is unlocking unprecedented opportunities for chip design. This presentation explores how Google Cloud Platform (GCP) empowers a new era of scalable and efficient workflows, drawing on insights and best practices honed from Alphabet's own internal use. While traditional on-premises EDA environments have served the industry well, GCP offers a transformative leap forward, enabling capabilities previously unattainable.

We'll showcase how GCP services like Google Kubernetes Engine (GKE) and Cloud Batch can handle the dynamic demands of chip design, optimizing data storage and analysis with services like Google Cloud Storage (GCS), and BigQuery. These services, battle-tested within Alphabet, provide the foundation for agile and responsive chip development. Furthermore, we'll discuss how value-added services built on GCP, including data solutions, runtime optimizations, and fine grain access control list (ACL) management, are critical for achieving next-generation chip design efficiency.

Speakers: Sathya Narasimhan, Google, US

EXPANDING THE TALENT POOL FOR IC DESIGN THROUGH EXPERIENTIAL LEARNING

Time: 11:15 AM - 12:00 PM

Topic Area(s): EDA

Session Type: TechTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: As the Global Advanced Electronics Industry becomes evermore ubiquitous, the demand for IC Designers is far outpacing the supply of Design talent entering the workforce. Mr. Hill will discuss the dynamics and challenges this presents to the education community. Driving awareness of the career and educational pathways needs to be integrated into secondary education, community college and early undergrad programs. Hands on and experential approaches will be discussed. A workshop platform has been developed to provide this early exposure and awareness to actual circuit design with access to an open source design platform and multi-project wafer fabrication and packaging. Survey results from multiple workshops will be presented.

Speakers: LaMar Hill, NY Design

LEVERAGING AI TO BOOST PRODUCTIVITY AND QUALITY OF RESULTS IN THE DIGITAL DESIGN CREATION FLOW

Time: 12:00 PM - 12:30 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Chip development schedules and costs have risen significantly especially for complex digital designs. Engineering teams face the challenge of achieving aggressive power, performance, area (PPA), and quality metrics in shorter schedule times, and with smaller teams.

AI has come a long way in EDA, from the initial machine learning applications to reinforcement learning, generative AI, and beyond. Technologies are in a breakthrough position in semiconductor design creation today, where AI-assisted EDA workflows are expected to lead to significantly higher productivity and better quality of results. AI can be prevalent in the digital design creation flow, providing tangible benefits to engineering in seamless and intuitive enhancements to the flow.

In this session, we will explore AI methods in the digital design creation flow. From enhancing High-Level Synthesis for accelerated design exploration, quantization analysis and PPA prediction, to accelerated RTL-to-GDS implementation flows that also produce better results, and employing AI techniques for improved fault isolation, we will discuss how AI is revolutionizing digital flows today, and how we can further leverage this exciting technology going forward.

Speakers: Ankur Gupta, Siemens

ACCELLERA-SPONSORED LUNCHEON: CAN AI CUT COSTS IN ELECTRONIC DESIGN & VERIFICATION WHILE ACCELERATING TIME-TO-MARKET?

Time: 12:00 PM - 1:30 PM

Session Type: Additional Meeting

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Join us for an insightful luncheon panel sponsored by Accellera, where industry leaders will discuss the transformative role of AI in semiconductor design and verification. As AI rapidly evolves, its potential to reduce costs, shorten time-to-market and address impending talent shortages is becoming increasingly evident—but what are the real-world opportunities and challenges?

This panel will bring together industry experts to share their vision and experiences, examining:

- The impact of AI on design and verification flows
- Envisioned benefits of applying AI, including cost reduction
- Challenges in training and deploying Large Language Models (LLMs), including IP ownership, ethics, and security
- The role of industry standards to shape AI-driven methodologies

The Accellera-sponsored luncheon is free to DAC attendees, but registration is required. Please visit https://www.accellera.org/news/events to register and find out more.

Speakers: Daniel Nenni, SemiWiki, US

POWERING THE FUTURE OF AI: ARE STANDARDS AN ENABLER OR A BOTTLENECK?: PANEL WITH COMPLIMENTARY LUNCH, SPONSORED BY SI2

Time: 12:00 PM - 1:00 PM

Topic Area(s): AI

Session Type: Additional Meeting

Room: 3016, Level 3

Description: As AI workloads scale dramatically, power, thermal management, and reliability have emerged as critical concerns. Industry standards such as IEEE 2416 and IEEE 1801 have attempted to address these issues through system-level power and thermal modeling. But are these standards accelerating innovation, or have they become a bottleneck for rapid technological advancement?

Powering the Future of AI features panelists from industry leaders in design and methodology for power and thermal optimization, including IBM and Cadence Design Systems. The lunch forum includes experienced leaders in the semiconductor industry and EDA standardization and targets system designers and architects, logic and circuit designers, validation engineers, CAD managers, researchers, and academicians.

Key discussion points include:

- Standards: Foundation or Constraint to Innovation in AI and system-level power management?
- Practical impacts and industry adoption: Real-world experiences from semiconductor foundries, AI hardware developers, and system integrators.
- Bridging Gaps: The role of emerging IEEE 2416 extensions (A/MS, thermal, multi-voltage) in addressing AI workloads.
- Cross-industry perspectives from EDA tool vendors, system integrators, and IP developers.
- How should standards evolve to effectively enable next-gen AI applications?

Speakers: Nagu Dhanwada, IBM, US

IEEE COUNCIL ON EDA DISTINGUISHED PANEL - 20TH ANNIVERSARY PANEL: AI HARDWARE & EDA, THE NEXT 20 YEARS: SMARTER, TALLER, DEEPER

Time: 12:00 PM - 1:30 PM

Session Type: Additional Meeting

Room: 3016/3018, Level 3

Moderator: Subhasish Mitra, Stanford University; L. Miguel Silveira, IST Tecnico / ULisboa

Speakers: Alberto Sangiovanni-Vincentelli, University of California, Berkeley; Vamsi Boppana, Advanced Micro Devices (AMD); Kunle Olokutun, SambaNova Systems Inc

NEW INNOVATION FRONTIER WITH LARGE LANGUAGE MODELS FOR SOC SECURITY

Time: 1:00 PM - 1:45 PM

Session Type: SKYTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: As complex SoCs become prevalent in virtually all systems, these devices also present a primary attack surface. The risks of cyberattacks are real, and AI is making them more sophisticated. As we also deploy AI into the SoC design process, it is imperative that secure design practices are incorporated as well.

Existing security solutions are inadequate to provide effective verification of complex SoC designs due to their limitations in scalability, comprehensiveness, and adaptability. Large Language Models (LLMs) are celebrated for their remarkable success in natural language understanding, advanced reasoning, and program synthesis tasks.

Recognizing this opportunity, we propose leveraging the emergent capabilities of Generative Pre-trained Transformers (GPTs) to address the existing gaps in SoC security, aiming for a more efficient, scalable, and adaptable methodology. In this presentation we offer an in-depth analysis of existing work, showcasing achievements, prospects, and challenges of employing LLMs in SoC security design and verification tasks.

Speakers: Mark Tehranipoor, University of Florida, Caspia Technologies

OPENACCESS COALITION FORUM: COMPLIMENTARY LUNCH, SPONSORED BY SI2

Time: 1:00 PM - 2:45 PM

Session Type: Additional Meeting

Room: 3016, Level 3

Description: As AI rapidly evolves, its potential to reduce costs, shorten time-to-market and address impending talent shortages is becoming increasingly evident—but what are the real-world opportunities and challenges?

This panel will bring together industry experts to share their vision and experiences, examining:

- The impact of AI on design and verification flows
- Envisioned benefits of applying AI, including cost reduction
- Challenges in training and deploying Large Language Models (LLMs), including IP ownership, ethics, and security
- The role of industry standards to shape AI-driven methodologies

The Accellera-sponsored luncheon is free to DAC attendees, but registration is required. Please visit https://www.accellera.org/news/events to register and find out more.

- **OpenAccess Coalition Forum: Complimentary Lunch, Sponsored by Si2**

  Andy Graham, Si2, Inc., US; Aki Fujimura, Design 2 Silicon, US; Yong-Hwan Jeon, SK-hynix, KR; Ed Gernert, Frontier Design, US; Larg Weiland, PDF Solutions Inc., US; Rhett Davis, North Carolina State University, US; Marshall Tiner, Si2, Inc., US

ARRIVAL PATHWAYS FOR CROSSING THE CHIP-N-PACKAGE ROUTES

Time: 1:30 PM - 3:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2012, Level 2

Description: Learn the routing strategies to cross the maze of chip to packaged parts delivery - keeping the clocks aligned to finding ways around crowded area or feeding throughs that cut the walls. Get Set and GO!

- **A Novel Feedthrough Insertion Methodology for Hierarchical SOC Designs: Achieving Reduction in Die Area**

  Rajanikant Sakariya, Subhadeep Aich, Vivek Joshi, Texas Instruments, IN; Roger Griesmer, Texas Instruments, US
- **ML Based PPA Push Using XAI**

  Kyoungsun Cho, Mintae Lee, jungho Kim, Sungyoul Seo, Kibum Nam, Bonghyun Lee, Ki-Ok Kim, Samsung, KR
- **Routing Congestion Mitigation Techniques Targeting Dense Designs**

  Nancy Zhou, Lakshmi Reddy, Alex Suess, Bijian Chen, Nathaniel Hieter, IBM, US
- **Efficient Automation Strategy for Package Substrate Routing**

  Keng Tuan Chang, Chih Yi Huang, Chen Chao Wang, Chin Pin Hung, Advanced Semiconductor Engineering, Inc., TW; Woei Haur Hung, Ting-Chi Wang, National Tsing Hua University, TW
- **Deterministic On Chip Variation Modeling of Clock Mesh**

  Tusharkant Mishra, Pradeep Kothari, Ayan Datta, Western Digital India Private Limited, IN
- **Dynamic Optimization of Skew Balancing through an Innovative Correct-by-Construct Path Delay Query Technique**

  Tejas Salunkhe, Subhadeep Aich, Abhranil Bose, Texas Instruments, IN

Session Chair(s): Patricia Fong, Marvell Technology

FORMAL AND STATIC VERIFICATION: STOP BUGS BEFORE THEY THINK THEY'RE INVITED

Time: 1:30 PM - 3:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2010, Level 2

Description: Static and formal based flows/solutions provide a bottom-up verification approach, helping engineers find certain class of bugs in the shortest time and helping manage efficient distribution of load across all verification technologies. In this session, presenters will share their experiences on applications like data path validation, formal verification, and metastability analysis (CDC/RDC).

- **Taming Formal to Define the Verification Quality**
  Surinder Sood, Kishan Mushar, Arm Ltd., GB
- **Formal Property Verification on Xeon SoC owned IPs**
  Prakeerthi Jallipalli, Intel Corporation, US
- **Identifying Soft-Resets in Design using RDC Tool Flow**
  Megha Hansaliya, Sushovan Kunti, Google, IN
- **Formal Signoff for Cross-Module Design Logic: A Novel Approach to Manage Formal Scope in Increasingly Complex Systems**
  Sai Asrith Tabdil, Sakthivel Ramaiah, Clarice Oliveira, Sorna Inian, Cadence Design Systems, Inc., US
- **Efficient Reset Metastability SignOff Methodology**
  Rangarajan Govindan, Intel Corporation, IN; Vikas Sachdeva, Saurav Choudhary, Real Inten, IN
- **Comprehensive Interconnect Verification – Leveraging Formal Methodology & Automation for verifying Address Decoding and Arbiter Verification, Performance Analysis**
  Kumar Singh, Parthasarathy Ramesh, Ayush Jodh, Harish Maruthiyodan, Texas Instruments, IN

Session Chair(s): Vikas Sachdeva, Real Intent

LLM INNOVATIONS: MIRAGE OR MILESTONE?

Time: 1:30 PM - 3:00 PM

Topic Area(s): Systems and Software

Session Type: Engineering Track

Room: 2008, Level 2

Description: The revolution brought about by LLM-based AI has disrupted our daily routines and significantly altered our expectations. The rapid pace of innovation in the world of LLMs has continually reshaped our outlook. Each time our applications hit a limitation, a new iteration quickly emerged, reigniting our AI aspirations and raising our expectations once more.

Are we merely chasing the AI dream like the proverbial 'chasing the carrot'? Have we already begun to reap the benefits, are we nearing the fulfillment of its promise, or are we simply engaging in a healthy exercise by pursuing it?

Drawing from real hands-on experience in this industry, where do you envision its future? What are your expectations, and how confident are you that it will meet them?

Our invited speakers will provide updates from the industry, showcasing clear examples of which investments have started to pay off, which were misguided, and how they foresee our world evolving in the near and distant future.

Session Chair(s): Monica Farkash, Advanced Micro Devices (AMD)

Moderator: Harry Foster, Siemens, US

Speakers: Romi Datta, DataRobot, US; Sean Sun, Samsung, US; Jay Bhadra, Advanced Micro Devices (AMD), US; Shahid Ikram, Marvell, US

AI MEETS SILICON: TRANSFORMING HARDWARE DESIGN THROUGH AI-DRIVEN INNOVATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: The integration of generative AI into EDA is ushering in a new era of hardware innovation. This session explores cutting-edge advancements in the application of machine learning models, particularly Large Language Models (LLMs), to hardware design automation and quantum code generation. The session begins with presentations on automating hardware design using LLMs. The discussion shifts to the potential of foundation models in enhancing EDA, followed by a novel approach to quantum code generation through LLMs. The session further delves into the use of diffusion models for generating synthetic RTL circuits, and concludes with the introduction of a multi-layered, hierarchical dataset to support machine learning in hardware design.

- **Free and Fair Hardware: A Pathway to Copyright Infringement-Free Verilog Generation using LLMs**
  Samuel Bush, Matthew DeLorenzo, Phat Tieu, Jeyavijayan Rajendran, Texas A&M University, US
- **Hardware Generation with High Flexibility using Reinforcement Learning Enhanced LLMs**
  Yifang Zhao, Hijie Li, Yi-Xiang Hu Yier Jin, University of Science and Technology of China, CN; Weimin Fu, Xiaolong Guo, Kansas State University, US
- **NetTAG: A Multimodal RTL-and-Layout-Aligned Netlist Foundation Model via Text-Attributed Graph**
  Wenji Fang, Wenkai Li, Shang Liu, Yao Lu, Hongce Zhang, Zhiyao Xie, Hong Kong University of Science and Technology, HK

- **Enhancing LLM-based Quantum Code Generation with Multi-Agent Optimization and Quantum Error Correction**
  Charlie Campbell, Hao (Mark) Chen, Wayne Luk, Hongxiang Fan, Imperial College London, GB
- **SynCircuit: Automated Generation of New Synthetic RTL Circuits Can Enable Big Data in Circuits**
  Shang Liu, Jing WANG, Wenji Fang, Zhiyao Xie, Hong Kong University of Science and Technology, HK
- **PyraNet: A Multi-Layered Hierarchical Dataset for Verilog**
  Bardia Nadimi, Ghali Omar Boutaib, Hao Zheng, University of South Florida, US

Session Chair(s): Luis Guerra e Silva, IST Tecnico / ULisboa, INESC-ID; Yutaka Masuda, Nagoya University

ALL YOU CAN ROUTE BUFFET

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: Prepare for a feast of routing innovations. Timing-driven Steiner trees are explored in both a Pareto-optimal framework and as an oracle problem within timing-constrained global routing. A new global routing model replaces traditional edge-based resources with area-based resources, improving quality and adaptation to incremental design changes. Detailed routing is enhanced through a reinforcement learning-based window selection strategy for more targeted rip-up and reroute. Mr.TPL shows how to achieve superior triple patterning routing solutions. Finally, intra-cell routing is integrated with local detailed routing to enhance overall routing quality.

- **PatLabor: Pareto Optimization of Timing-Driven Routing Trees**
  Zhiyang Chen, Xia Yin, Tsinghua University, CN; Hailong Yao, University of Science and Technology Beijing, CN
- **Cost-Distance Steiner Trees for Timing-Constrained Global Routing**
  Stephan Held, Edgar Perner, University of Bonn, DE
- **Dynamic Local Usage: An accurate model for usage of tile-internal wiring in Global Routing**
  Daniel Blankenburg, Tilmann Bihler, University of Bonn, DE
- **Reinforcement Learning-Driven Window Selection for Enhanced Window-Based Rip-up and Reroute in Chip Detailed Routing**
  Yu-Chan Keng, Yu-Chun Pai, Yih-Lang Li, National Yang Ming Chiao Tung University, TW; Wen-Hao Liu, Haoxing Ren, Danny Liu, Rongjian Liang, Mark Ho, Anthony Agnesina, Nvidia, US
- **Mr.TPL: A New Multi-pin Routing Method for Triple Patterning Lithography**
  Chengkai Wang, Weiqing Ji, Mingyang Kou, Hailong Yao, University of Science and Technology, Beijing, CN; Zhiyang Chen, Tsinghua University, CN; Fei Li, Empyrean Technology, CN
- **TransRoute: A Novel Hierarchical Transistor-Level Routing Framework Beyond Standard-Cell Methodology**
  Chen-Hao Hsu, David Z. Pan, The University of Texas at Austin, US; Laurent Perron, Google, FR; Frédéric Didier, Google, FR; Xiaoqing Xu, Google, US; Hao Chen, Google, US

Session Chair(s): Michael Kazda, IBM; Stephan Held, University of Bonn, DE

FROM TEST TO SLM ADVANCED SOLUTIONS

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3006,Level 3

Description: This session covers a range of innovative solutions including, how to maximize the prediction accuracy for aging SRAMs; how to utilize machine learning in generating in-field self-test libraries; how to further optimize the performance of parallel fault simulation and test compaction; how to optimize the efficiency of NOCs under process variation; and how to improve the fault tolerance of the microfluidic MUXs.

- **Asymmetric Predictive Testing for Aging in SRAMs**
  Yunkun Lin, Mingye li, Sandeep Gupta, University of Southern California, US
- **Machine Learning-Driven STL Generation for Enhancing Functional Safety of E/E Systems**
  Sanjay Das, Swastik Bhattacharya, Anand Menon, Kanad Basu, The University of Texas at Dallas, US; Shamik Kundu, Arnab Raha, Suvadeep Banerjee, Suriya Natarajan, Intel Corporation, US; Pooja Madhusoodhanan, Prasanth Viswanathan Pillai, Rubin Parekhji, Texas Instruments, IN
- **EPICS: Efficient Parallel Pattern Fault Simulation for Sequential Circuits via Strongly Connected Components**
  Mingjun Wang, Jianan Mu, Xinyu Zhang, Bin Sun, Zizhen Liu, Feng Gu, Gao Jun, Shengwen Liang, Jing Ye, Xiaowei Li, Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN; Hui Wang, CASTEST, Beijing, CN; Yihan Wen, Beijing University of Technology, CN
- **PastATPG: A Hybrid ATPG Framework for Better Test Compaction with Partial Assignment SAT**
  Zhiteng Chao, Xindi Zhang, Xinyu Zhang, Jianan Mu, Zizhen Liu, Shengwen Liang, Shaowei Cai, Jing Ye, Xiaowei Li, Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN

- **Process-Variation-Aware Design Optimization for Wavelength-Routed Optical Networks-on-Chip**
  Liaoyuan Cheng, Mengchu Li, Tsun-Ming Tseng, Martin Schottenloher, Ulf Schlichtmann, Technical University of Munich, DE
- **FT-MUX: A Fault-Tolerant Microfluidic Multiplexer**
  Mengchu Li, Jiahui Peng, Tsun-Ming Tseng, Ulf Schlichtmann, Technical University of Munich, DE

Session Chair(s): Savita Banerjee, Meta; Jing-Jia Liou, National Tsing Hua University

LLM UPRISING: FAST & FURIOUS

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3002,Level 3

Description: The revolution brought about by LLM-based AI has disrupted our daily routines and significantly altered our expectations. The rapid pace of innovation in the world of LLMs has continually reshaped our outlook. Each time our applications hit a limitation, a new iteration quickly emerged, reigniting our AI aspirations and raising our expectations once more.

Are we merely chasing the AI dream like the proverbial 'chasing the carrot'? Have we already begun to reap the benefits, are we nearing the fulfillment of its promise, or are we simply engaging in a healthy exercise by pursuing it?

Drawing from real hands-on experience in this industry, where do you envision its future? What are your expectations, and how confident are you that it will meet them?

Our invited speakers will provide updates from the industry, showcasing clear examples of which investments have started to pay off, which were misguided, and how they foresee our world evolving in the near and distant future.

- **VEDA: Efficient LLM Generation Through Voting-based KV Cache Eviction and Dataflow-flexible Accelerator**
  Zhican Wang, Gang Wang, Zhenyu Li, Jianfei Jiang, Yanan SunGuanghui He, Shanghai Jiao Tong University, CN; Hongxiang Fan, Imperial College London, GB; Haroon Waris, Institute of Space Technology (IST), PK
- **LLMShare: Optimizing LLM Inference Serving with Hardware Architecture Exploration**
  Hongduo Liu, Peng Xu, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, HK; Chen Bai, The Hong Kong University of Science and Technology, CN; Lihao Yin, Xianzhi Yu, Hui-Ling Zhen, Mingxuan Yuan, Huawei, HK
- **SSDTrain: An Activation Offloading Framework to SSDs for Faster Large Language Model Training**
  Kun Wu, Jeongmin Park, Steve Lumetta, Wen-mei Hwu, University of Illinois at Urbana-Champaign, US; Xiaofan Zhang, Google, US; Mert Hidayetoğlu, Snowflake, US; Vikram Sharma Mailthody, Nvidia, US; Sitao Huang, University of California, Irvine, US
- **LEMOE: LLM-Enhanced Multi-Objective Bayesian Optimization for Microarchitecture Exploration**
  Jingyuan Li, Jianrong Zhang, Wenbo Yin, Lingli Wang, Fudan University, CN; Ye Li, University of New South Wales, Australia
- **SpecASR: Accelerating LLM-based Automatic Speech Recognition via Speculative Decoding**
  Linye Wei, Shuzhang Zhong, Songqiang Xu, Runsheng Wang, Ru Huang, Meng Li, Peking University, CN
- **PISA: Efficient Precision-Slice Framework for LLMs with Adaptive Numerical Type**
  Fangxin Liu, Ning Yang, Zongwu Wang, Shanghai Jiao Tong University, CN; Qingxiao Sun, China University of Petroleum, Beijing, CN; Liqiang Lu, Zhejiang University, CN

Session Chair(s): Shiyu Li, Nvidia; M. Hassan Najafi, University of Louisiana at Lafayette

QUANTUM BREAKTHROUGHS CREATING GAME-CHANGING APPLICATIONS

Time: 1:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3003, Level 3

Description: The session discusses game-changing applications of quantum computing in finance, community detection, computational advantages of quantum machine learning over classical models, quantum cryptanalysis, and developing distributed quantum computing for real-world applications. The first paper solves portfolio optimization problems in finance with the help of a novel design of an HHL quantum algorithm. Community detection is an important problem in network analysis; the second paper demonstrates the potential of hybrid quantum-inspired solutions for advancing community detection in large-scale graph data. The third paper shows that hybrid quantum neural networks provide a more scalable and resource-efficient solution over purely classical models, positioning them as a promising alternative for tackling complex computational problems. The fourth and fifth papers discuss novel quantum arithmetic circuits for quantum cryptanalysis with the help of measurement-based uncomputation and windowed arithmetic. Distributed quantum computing (DQC) offers a promising pathway for scaling up quantum computing; therefore, the sixth paper discusses hardware-software co-design for DQC systems, paving the way for more practical and efficient implementations for real-world applications.

- **SAPO: Improving the Scalability and Accuracy of Quantum Linear Solver for Portfolio Optimization**
  Tianze Zhu, Liqiang Lu, Jiajun Chen, Hengrui Chen, Meng Xi, Jinshan Zhang, Jianwei Yin, Zhejiang University, CN; Yuhang Chen, Peking University, CN; Xiaoming SUN, Institute of Computing Technology, Chinese Academy of Sciences
- **Scalable Community Detection Using QHD and QUBO Formulation**
  Jinglei Cheng, Junyu Liu, The University of Pittsburgh, US; Ruilin Zhou, Yuhang Gan, Chen Qian, University of California, Santa Cruz, US
- **Computational Advantage in Hybrid Quantum Neural Networks: Myth or Reality?**
  Muhammad Kashif, Alberto Marchisio, Muhammad Shafique, New York University Abu Dhabi, UA
- **Measurement-based Uncomputation of Quantum Circuits for Modular Arithmetic**
  Alessandro Luongo, Center for Quantum Technologies (CQT), SG; Antonio Michele Miti, Sapienza Universit`a di Roma, IT; Varun Narasimhachar, Agency for Science, Technology and Research (A*STAR), SG; Adithya Sireesh, University of Edinburgh, GB
- **Optimizing Windowed Arithmetic for Quantum Attacks against RSA2048**
  Alessandro Luongo, Center for Quantum Technologies (CQT), SG; Varun Narasimhachar, Agency for Science, Technology and Research (A*STAR), SG; Adithya Sireesh, University of Edinburgh, GB
- **Hardware-Software Co-design for Distributed Quantum Computing**
  Ji Liu, Paul Hovland, Argonne National Laboratory, US; Allen Zang, Tian Zhong, University of Chicago, US; Martin Suchara, Microsoft, US

Session Chair(s): Saurabh Kotiyal, Altera; Sanjaya Lohani, Southern Methodist University

THE "AUTO" IN AUTONOMOUS SYSTEMS

Time: 1:30 PM - 3:00 PM

Topic Area(s): Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: This session showcases innovations that put the "auto" in autonomous systems. Topics include real-time LiDAR odometry, event-based sensing, EEG-controlled prosthetics, safe controller synthesis, mutation testing and hyperparameter tuning for efficient computing. Whether it's enhancing autonomy in robotics, cyber-physical systems, or AI-driven hardware, this session explores cutting-edge research shaping the future of intelligent, self-sustaining systems.

- **LIO-DPC: Accurate and Fast LiDAR-Inertial Odometry with Dynamic Pose Chain**
  Yuexin Mu, Ao Ren, Duo Liu, Zihao Zhang, Haojie Lu, Longyi Zhou, Huachen Tan, Kan Zhong, Yujuan Tan, Chaoxia Qin, Chongqing University, CN
- **Espresso: Exploiting the Sparsity Property in Event Sensors with Spatiotemporal Ordering**
  Leshan Li, Hongyi Li, Qingyuan Yang, Mingtao Ou, Rong Zhao, Xinglong Ji, Tsinghua University, CN
- **CognitiveArm: Enabling Real-Time EEG-Controlled Prosthetic Arm Using Embodied Machine Learning**
  Abdul Basit, Maha Nawaz, Saim Rehman, Muhammad Shafique, New York University, Abu Dhabi, AE
- **Learning-Aided Safe Controller Synthesis with Formal Guarantees via Vector Barrier Certificates**
  Xia Zeng, Southwest University, CN; Mengxin Ren, Zhengfeng Yang, East China Normal University, CN; Zhiming Liu, Southwest University, CN
- **Live Region Mutation Testing for Commercial Cyber-Physical System Development Tool Chain**
  Lehuan Zhang, Xiaochen Li, He Jiang, Dalian University of Technology, CN; Shikai Guo, Zixuan Wang, Xiaoyu Wang, Dalian Maritime University, CN
- **A Proxy-Free Online Hyperparameter Optimization Framework for ISP Hardware System**
  Jiaming Liu, Xuan Huang, Ruoxi Zhu, Qi Zheng, Shuocheng Wang, Shushi Chen, Chang Liu, Jun Tao, Yibo Fan, Fudan University, CN; Zhijian Hao, Xidian University, CN; Leilei Huang, East China Normal University, CN

Session Chair(s): Abhinav Goel, Nvidia; Oliver Bringmann, University of Tüebingen, DE

TURBOCHARGING DEEP LEARNING TRAINING: EFFICIENCY MEETS INNOVATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000,Level 3

Description: This session covers advancements in optimizing deep learning training and inference, with a focus on edge-device performance, low-precision training, neuromorphic computing, and hardware-software co-design. The papers presented here explore efficient techniques that reduce model complexity, energy consumption, and improve robustness, enabling better performance for edge and specialized systems.

- **NoiseZO: RRAM Noise-Driven Zero-Order Optimization for Efficient Forward-Only Training**
  Shuqi Wang, Zhengwu Liu, Chenchen Ding, Chen Zhang, Taiqiang Wu, Jiajun Zhou, Ngai Wong, The University of Hong Kong, HK
- **APSQ: Additive Partial Sum Quantization with Algorithm-Hardware Co-Design**
  Yonghao Tan, Pingcheng Dong, Yongkun Wu, Yu Liu, Xuejiao Liu, Peng Luo, Shih-Yang Liu, Xijie Huang, Dong Zhang, Luhong Liang, Kwang-Ting Cheng, The Hong Kong University of Science and Technology, CN

- **NN-AdderNet: Nonnegative and Sparse Weight Optimization for Ultra-Low Bitwidth AdderNet Quantization and Compression**
  Yunxiang Zhang, Wenfeng Zhao, Binghamton University, US; Gengchen Sun, Lizhi Fang, Biao Sun, Tianjin University, CN
- **Replay4NCL: An Efficient Memory Replay-based Methodology for Neuromorphic Continual Learning in Embedded AI Systems**
  Mishal Minhas, Falah Awwad, United Arab Emirates University, AE; Rachmad Vidya Wicaksana Putra, Muhammad Shafique, New York University, Abu Dhabi, AE; Osman Hasan, National University of Sciences and Technology, PK
- **FF-INT8: Efficient Forward-Forward DNN Training on Edge Devices with INT8 Precision**
  Jingxiao Ma, Sherief Reda, Brown University, US; Priyadarshini Panda, Yale University, US
- **BirdMoE: Reducing Communication Costs for Mixture-of-Experts Training Using Load-Aware Bi-random Quantization**
  Donglei Wu, Guangzhou University, CN; Weihao Yang, Xiangyu Zou, Wen Xia, Harbin Institute of Technology, CN; Jinda Jia, Indiana University, US; Dingwen Tao, Institute of Computing Technology, Chinese Academy of Sciences, CN; Zhihong Tian, Guangzhou University, CN

Session Chair(s): Fan Yang, Fudan University; Li Shang, Fudan University

SECURITY FOR/WITH HARDWARE – (WHY) HAVEN'T WE ALREADY SOLVED THIS?

Time: 1:30 PM - 3:00 PM

Session Type: Research Panel

Topic Area(s): Security

Room: 3012, Level 3

Description: With the rise in interconnected devices and digitization of systems ranging from consumer products to critical infrastructure, there are increased demands for hardware as the foundation for system security. Trust is critical. Recent efforts include the Hardware Common Weakness Enumerations (HW-CWEs), the IEEE P3164 effort (for security annotation of IP), and others. Handling throughout the design lifecycle, such as security design, implementation, verification, and validation, seems a daunting task. So, where are we in the state-of-the-art of hardware security? What are the barriers that prevent research innovations from making it prime time? What problems haven't we solved yet? Why are we severely witnessing increasingly discovered hardware vulnerabilities in terms of number and sophistication?

Organizer(s): Tuba Yabuz, University of Florida; Jason Fung, Intel Corporation

Moderator: Benjamin Tan, University of Calgary, CA

Speakers: Ahmad-Reza Sadeghi, Technische Universität Darmstadt, DE; Jeyavijayan Rajendran, Texas A&M University, US; Warren Savage, University of Maryland, US; Sharad Malik, Princeton University, US; Farinaz Koushanfar, University of California, San Diego, US

ON THE LIMITATIONS OF VLSI STRUCTURAL MANUFACTURING TEST AND FUTURE DIRECTIONS

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: Structural testing has been very successful in the VLSI manufacturing process to screen out faulty devices and provide high outgoing product quality. However, recent reported data from Google and Meta show that faulty chips are escaping the test programs and ending in causing serious trouble in field; e.g., Silent Data Corruptions (SDC). Meta recently reported at International Test Conference 2024 that approximately 78% of in field interruptions are attributed to confirmed hardware issues such faulty GPUs, faulty memories, etc. This calls for immediate improvements of used fault models and test patterns at manufacturing test.

This session addresses the limitations of existing fault models and test generation, and highlights further direction for better fault modelling; both for logic and memory. The first talk shows the limitations of (commercial) existing solutions. For example, reliance on the stuck-at fault model persists even though data extracted from the test literature reveals that the percentage of defects that exhibit stuck-at fault behaviour has significantly reduced over the years; real data measurements will be provided to support statement. The second talk shows how increasing random process variations in advanced low-nanometer nodes are introducing timing marginalities that can cause unpredictable failures under adverse operating conditions; such marginalities are not considered during test generation for structural manufacturing tests yet. Consequently it is not detected by currently used industrial test programs leading to a significant number of test escapes. The third talk presents Device-Aware-Test; a new approach that aims at closing the gap between fault models and real defects. The approach is demonstrated on an industrial STT-MRAM design.

- **Incompatible: Test Quality and Fortuitous Detection**
  Shawn Blanton, Carnegie Mellon University, US
- **Enhancing Test Quality by Targeting Timing Marginalities Due to Process Variations**
  Adit Singh, Auburn University, US

- **Device-Aware Test: A Means to Attack Unmodeled Defects**
  Said Hamdioui, Delft University of Technology, NL

Organizer(s): Mottaqiallah Taouil, Delft University of Technology, NL

COVERAGENT: HOW AGENTIC AI IS REDEFINING FUNCTIONAL COVERAGE CLOSURE

Time: 1:45 PM - 2:15 PM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Functional coverage closure remains one of the most persistent and resource-intensive challenges in RTL verification. Despite decades of EDA tool evolution, coverage gaps often require manual analysis, ad hoc scripting, and repeated testbench iterations. In this talk, we introduce CoverAgent, an agentic AI system purpose-built to identify, target, and close the last functional coverage gaps that conventional tools and workflows leave behind.

CoverAgent operates as an autonomous agent within your existing verification environment. It analyzes coverage reports, understands testbench structure, infers unreachable states, and autonomously proposes targeted stimuli and constraint adjustments — all without rewriting your entire environment. Built on a foundation of LLMs and agent-based reasoning, CoverAgent bridges the usability gap between design intent and simulation behavior.

We present real-world case studies demonstrating how CoverAgent accelerated closure by 80% in complex SoC environments, uncovered unreachable bins missed by traditional tools, and improved the productivity of design verification engineers without sacrificing control or interpretability.

Whether you're building CPUs, accelerators, or memory subsystems, CoverAgent fits seamlessly into your UVM or SystemVerilog flow. It complements existing commercial tools, providing a new dimension of intelligence to the verification loop.

Join us to see how agentic AI can supercharge your coverage strategy, reduce manual effort, and make coverage closure not just achievable — but efficient, scalable, and even enjoyable.

Speakers: Mehir Arora, Zackary Glazewski, William Wang, ChipAgents.ai, US

BREAKING THE DESIGN AUTOMATION MOLD; WILD AND CRAZY IDEAS FOR GLOBAL OPTIMIZATION

Time: 2:00 PM - 2:45 PM

Topic Area(s): EDA

Session Type: DAC Pavilion Panel

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The CHIPS Act is a game-changer for the U.S. semiconductor industry, extending beyond manufacturing to fuel innovation in design enablement and IP development. Through strategic investments in programs like the National Semiconductor Technology Center (NSTC), the National Advanced Packaging Manufacturing Program (NAPMP), and the Microelectronics Commons, the Act supports cutting-edge EDA tools, semiconductor IP, and next-generation design infrastructure. These efforts are critical to strengthening U.S. leadership in semiconductor R&D and reducing reliance on foreign technologies.

This panel will explore how CHIPS Act investments foster next-generation design methodologies, AI-driven automation, and cloud-enabled collaboration platforms, ensuring that U.S. semiconductor design remains competitive. Experts from government and industry will discuss the role of Natcast /National Semiconductor Technology Center(NSTC) in accelerating research with prototype programs such as AIDRFIC, which is driving advancements in semiconductor innovation. The discussion will highlight how these initiatives strengthen domestic design capabilities, support startups, academic institutions, and industry partnerships, and reduce reliance on foreign technologies to create a resilient and globally competitive semiconductor ecosystem.

Organizer(s): Nagesh Gupta, Ilmda.ai

Moderator: Bernard Murphy, SemiWiki

Speakers: Gopal Iyer, Lattice Semiconductor; Vidya Rajagopalan, Rivian; Rajesh Kashyap, Ericsson; Amit Dhir, PWC

THE RENAISSANCE OF EDA STARTUPS

Time: 2:30 PM - 3:15 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: For decades, the EDA industry has been dominated by a few major players, creating high barriers to entry. Yet, a remarkable shift is underway. In the past two years, a wave of EDA startups has emerged, securing significant venture funding and gaining customer traction. This resurgence is often driven by AI/ML advancements, new semiconductor design challenges, and evolving market dynamics.

This panel brings together key stakeholders to discuss:

- Market drivers: What conditions and breakthroughs are fuelling this startup boom?
- Innovation focus: How are startups identifying market opportunities and leveraging AI to solve complex design problems?
- Funding trends: How have investor attitudes toward deep tech and EDA evolved?
- Industry dynamics: How are startups navigating relationships with established players and potential acquirers?
- Success strategies: What's working in customer acquisition, differentiation, and scaling?

Our panel features EDA entrepreneurs, venture capitalists, and industry leaders shaping this transformation. Join us for an insightful discussion on the future of EDA innovation and the opportunities ahead.

Speakers: Moshe Zalcberg, Veriest, Silicon Catalyst, IS; Priyanka Mathikshara, Voltai, US; Kanu Gulati, Khosla Ventures, US; Brian Schechter, Primary Venture Partners, US; Vinod Kariat, Cadence Design Systems, Inc., US

AI AND VLSI: A SYMBIOTIC REVOLUTION ENRICHING OUR LIVES AND SHAPING OUR FUTURE

Time: 3:00 PM - 3:45 PM

Topic Area(s): AI

Session Type: DAC Pavilion Panel

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The recent AI revolution has dramatically reshaped computing, with VLSI technology playing a crucial role. This panel aims to unite industry and academic leaders to explore the symbiosis between AI and VLSI, highlighting how each fuels advancements in the other. We will discuss AI's role in driving innovations in VLSI and computer hardware, from specialized AI chips to advanced architectures, faster I/O, and increased memory capacities. Conversely, we will explore how VLSI advancements, such as GPUs and custom AI accelerators, power AI's rapid growth. As AI permeates EDA tools, we will examine its potential to revolutionize chip design, optimizing performance, power, and time-to-market. We will also debate whether hardware's slower development pace compared to software has hindered or paradoxically benefited AI's progress. The panel will address AI's sustainability challenges, questioning if next-gen hardware can meet AI's massive computational demands sustainably or exacerbate energy consumption and environmental impacts. Through this panel, we would like to inspire future VLSI pioneers, especially women and young engineers, by showcasing cutting-edge AI-VLSI synergies and igniting creativity to redefine technological frontiers. Join us to explore how these interconnected fields collaboratively shape computing's future.

Moderator: Ramune Nagisetty, NatCast, US

Speakers: Manoj Selva, Intel Corporation, US; Sidney Tsai, IBM, US; Arijit RayChowdhury, Georgia Institute of Technology, US; Vijay Raghunathan, Purdue University, US; Rob Aitken, U.S. Department of Commerce, US

ACCELERATING TAPEOUT BY MONTHS WITH COST-EFFECTIVE PER-MINUTE EDA CLOUD LICENSING

Time: 3:30 PM - 4:00 PM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: In this session, we will present how we optimized SPICE simulation for a D flip-flop, reducing the transient analysis Monte Carlo simulation time for 5000 samples to under 1 hour from the typical 8-hour run, while simultaneously reducing EDA software license costs by 75% on the cloud. We then leveraged the same technique to scale to larger designs with more complex requirements, achieving similar results and accelerating speedup 2X to 52X across multiple flows such as timing and power signoff, formal verification, and DRC extraction. We will share specific real-world design scenarios and examples of successful tapeouts completed months ahead of schedule by scaling per-minute licensing usage across the entire chip design project.

Panelists: Vikram Bhatia, Sridhar Panchapakesan, Synopsys

AI AND CHIPLET/MULTI-DIE: VERIFICATION SCALABILITY AND AI DRIVEN AUTOMATION

Time: 3:30 PM - 5:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2010, Level 2

Description: Chiplet based design demands scalability and AI can provide multifold gains in productivity by automating flows and providing new solutions. In this session, presenters will share their insights into flows/methodology for Chiplet based design and how AI can be leveraged to transform the verification landscape.

- **Enhancing Verification Throughput in Random Tests Regression with a Novel Machine Learning Engine**
  Davide Sanalitro, STMicroelectronics, IT
- **Expediting UCIe and Boot Verification using Distributed Ndie Simulations and Emulation for Multi-Chiplet AI SoCs**
  Harshal Kothari, Jerin Jose, Jasobanta Sahoo, Ayush Agrawal, Madhukar Ramegowda, Samsung Semiconductor, IN

- **Revolutionizing Digital ASIC Design Through AI**
  Paulo Magno, Ricardo Araujo, Miguel Caetano, Mara Carvalho, Luis Cruz, Synopsys, PT; Luis Francisco, Synopsys, US
- **A Leap Forward in Formal Verification Using Generative AI**
  Shahid Ikram, Marvell Semiconductor, US; Sean Safarpour, Alex Chang, Synopsys, US
- **An Automated and Scalable Monitor-and-Checker Solution for SMMU Verification in Multi-Die SoCs**
  Junha Jeon, Namyoung Kim, Hyunman Park, Jaein Hong, Moonki Jun, Sanghune Park, Samsung, KR
- **Fear Not! With LLMs, Learning PSS Isn't Scary At All**
  Tom Fitzpatrick, Dan Yu, Siemens, US; Mohamed Moselhy, Sarah Hesham, Mohamed Nafea, Waseem Raslan, Siemens, EG

Session Chair(s): Haoxing "Mark" Ren, Nvidia

COMPLETE YOUR POWER AND THERMAL ENVELOPES WITH SECURITY AND PREDICTABILITY

Time: 3:30 PM - 5:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2012, Level 2

Description: Keep your cool while removing heat and not revealing your secrets to performance and security. This season deliver secure designs that dont melt down.

- **A Hybrid Simulation Technique for High-Speed and Accurate System-Level Side-Channel Leakage Analysis**
  Kazuki Monta, Secafy Co., Ltd., JP; Takafumi Oki, Rikuu Hasegawa, Takuya Wadatsumi, Takuji Miki, Makoto Nagata, Kobe University, JP; Lang Lin, Norman Chang, Ansys, US
- **Thermal Characteristic Analysis of Back-Side Power Delivery Network**
  Sunggu Kang, Samsung, KR
- **3DIC Thermal-Aware Early Design Optimization**
  Chia-Yi Liou, Chih-Hsiang Yang, Kuan-Ting Kuo, Intel Corporation, TW; Chung-Ching Peng, Venkatesh Ramamurthy, Vivek Rajan, Intel Corporation, US; Narender Akilla, Naresh Mummidivarapu, Yashodhara Tarey, Kumar Subramani, Cadence Design Systems, Inc., US
- **Mitigation of Functional Power Dissipation in Parasitic Scan Shift Test Buffers**
  Aradhana Kumari, STMicroelectronics, FR; Ankur Bal, STMicroelectronics, IN
- **PPA Evaluation of BS-PDN Compared to FS-PDN in the Early Stage**
  Dean Huang, Intel Corporation, TW; Andy Wei, Chee How Lim, Intel Corporation, US
- **A Simulation Technique of Thermal Side-Channels from Cryptographic Circuits**
  Shuhei Yokota, Kobe University, JP; Rikuu Hasegawa, Kobe University, JP; Kazuki Monta, Kobe University, JP; Takaaki Okidono, Kobe University, JP; Takuji Miki, Kobe University, JP; Makoto Nagata, Kobe University, JP

Session Chair(s): Amol Joshi, Intel Corporation

SOFTWARE DEVELOPMENT & AI APPLICATIONS

Time: 3:30 PM - 5:00 PM

Topic Area(s): Systems and Software

Session Type: Engineering Track

Room: 2008, Level 2

Description: This session delves into cutting-edge methodologies and frameworks revolutionizing system-on-chip (SoC) development, software optimization, and artificial intelligence collaboration. Explore advanced hybrid emulation techniques that accelerate Android home screen bring-up and system software validation at the pre-silicon stage, reducing time-to-market and debugging complexities. Discover innovative power-saving strategies for embedded devices, including the use of accelerated RAM (XRAM) for efficient warm boots, optimizing system response times and battery life. Learn about the Coreless Test Framework (CTF), a simplified verification method enhancing virtual platform accuracy in early development stages. The session also introduces TrustChain, a decentralized AI framework leveraging IOTA Tangle and Matrix for secure, consensus-driven multitasking, addressing privacy and scalability challenges. Lastly, gain insights into rom-based automotive boot codes compliant with functional safety and cybersecurity standards, critical for software-defined vehicles managing real-time tasks and high-performance applications. Join us to explore these advancements and their impact on the future of SoC development and AI applications.

- **Accelerated SoC Level Android Home Screen Bring-up, System Software Development and Validation at Pre-Silicon with Advanced Hybrid Emulation Methodology**
  Rinkesh Yadav, Sarang Kalbande, Naushad Kollikkara, Garima Srivastava, Samsung Semiconductor, IN; Hyundon Kim, Samsung, KR
- **Enhanced Power Saving with System-on-Chip and Software Design Optimization**
  Bhargavi Kandala, Omkar Singh, Thejeswara Reddy, Prasad Dandra, Somraj Mani, Tushar Vrind, Samsung Semiconductor, IN; Seokha Hong, Samsung, KR
- **Improving Functional Accuracy of Virtual Platform Based on Coreless Test Framework in Early Development Stage**
  Jaeyeong Jeon, Sangwoo Han, Jooho Wang, Seungik Ha, Jinbeom Kim, Myeongjin Kim, Jongseong Park, Kyungsu Kang, Silwan Chang, Samsung, KR
- **TrustChain: Enabling Consensus-Driven Multitasking AI**
  Arpita Sarker, Hochschule Heilbronn, DE
- **Rom-Based Automotive Boot Code, in Compliancy with Functional Safety and Cbersecurity Standards**
  Blpul Halder, Davide Fiorese, Neha Saxena, Agata Notario, Simone Colle, STMicroelectronics, IN

Session Chair(s): Jakob Engblom, ASTC

BACK TO THE FUTURE: WHERE SPEED MEETS EFFICIENCY

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002,Level 3

Description: This session explores cutting-edge advancements in hardware acceleration, focusing on optimizing computation, memory access, and parallelism in modern architectures. Featuring research on heterogeneous reconfigurable accelerators and FPGA optimization, the papers highlight novel approaches to accelerating key computational tasks. Topics include efficient sparse matrix multiplication, inter-tile parallelism, adaptive tree computations, large number modular reduction, compiler mapping strategies for CGRAs and physical design for nonvolatile FPGAs. Together, these works demonstrate how innovations in hardware and algorithm design are driving the future of high-performance computing, pushing the boundaries of speed, efficiency, and scalability in diverse applications.

- **HeteroSVD: Efficient SVD Accelerator on Versal ACAP with Algorithm-Hardware Co-Design**
  Xinya Luan, Kai Shi, Jianwang Zhai, Kang Zhao, Beijing University of Posts and Telecommunications, CN; Zhe Lin, Sun Yat-sen University, CN
- **VSpGEMM: Exploiting Versal ACAP for High-Performance SpGEMM Acceleration**
  Kai Shi, Xinya Luan, Jianwang Zhai, Kang Zhao, Beijing University of Posts and Telecommunications, CN; Zhe Lin, Sun Yat-sen University, CN
- **HiSpTRSV: Exploring Tile-Level Parallelism for SpTRSV Acceleration on FPGAs**
  Fan Sun, Fang Dong, Dian Shen, Southeast University, CN
- **A Data-Centric Hardware Accelerator for Efficient Adaptive Radix Tree**
  Jin Zhao, Yu Zhang, Jun Huang, Weihang Yin, Hui Yu, Hao Qi, Zixiao Wang, Xiaofei Liao, Hai Jin, Huazhong University of Science and Technology, CN; Longlong Lin, Southwest University, CN
- **ALLMod: Exploring \underline{A}rea-Efficiency of \underline{L}UT-based \underline{L}arge Number \underline{Mod}ular Reduction via Hybrid Workloads**
  Fangxin Liu, Haomin Li, Zongwu Wang, Li Jiang, Shanghai Jiao Tong University, CN; Bo Zhang, Mingzhe Zhang, Shoumeng Yan, Ant Group, CN
- **GPS: GNN-Based Two-Stage Pre-Scheduling Loop Mapping Method on CGRAs**
  Mingyang Kou, Weiqing Ji, Hailong Yao, University of Science and Technology, Beijing, CN; Shouyi YIN, Tsinghua University, CN
- **Rewire: Advancing CGRA Mapping Through a Consolidated Routing Paradigm**
  Zhaoying Li, Dan Wu, Dhananjaya Wijerathne, Dan Chen, Huize Li Tulika Mitra, National University of Singapore, SG; Cheng Tan, Google, US
- **Routability-Aware Packing for High-density Nonvolatile FPGAs**
  Huichuan Zheng, Yuqing Xiong, Jian Zuo, Hao Zhang, Zhenge Jia, Mengying Zhao, Shandong University, CN

Session Chair(s): Tianhao Cai, Beihang University, CN; Dirk Stroobandt, Ghent University, BE

BREAKTHROUGHS IN VLSI: POWER-EFFICIENT AI AND REVOLUTIONARY CIRCUITRY

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3003, Level 3

Description: This session brings together groundbreaking research and innovative advancements in the fields of VLSI design, power efficiency, AI-driven design automation, and advanced circuitry. The goal is to explore and discuss the latest developments that are pushing the boundaries of technology, circuits, and systems. The session presents topics on DNN accelerators, AI-driven design automation, and innovations in analog circuit design. The session also covers new energy efficient technologies in digital design, including probabilistic quantum tunneling for robotic perception and multifunctional backside metal layers, as well as energy-efficient solutions for RISC-V cores and video coding. It provides a comprehensive overview into the challenges, methodologies, and breakthroughs shaping the future of semiconductor technology and electronic design.

- **EPIC: Error PredIction and Correction for Power-Efficient Voltage Underscaling Multiply-Accumulate Unit**
  Tongjing Wu, Xiaolu Hu, Tong Li, Hui Wang, Weifeng He, Zhigang Mao, Honglan Jiang, Shanghai Jiao Tong University, CN; Siting Liu, ShanghaiTech University, CN;
- **PoP-ECC: Robust and Flexible Error Correction against Multi-Bit Upsets in DNN Accelerators**
  Taewon Park, Dongwhee Kim, Samsung, KR; Saeid Gorgin, Jaeho Shin, Jungrae Kim, Sungkyunkwan University, KR; Michael Sullivan, Nvidia, US
- **AdreamDCO: AI-Driven Robust and Efficient Design Automation for Digitally Controlled Oscillators**
  Yaolong Hu, Hao Guo, Jiaqi Liu, Taiyun Chi, Rice University, US; Shikai Wang, Weidong Cao, George Washington University, US

- **EVA: An Efficient and Versatile Generative Engine for Targeted Discovery of Novel Analog Circuits**
  Jian Gao, Xuan Zhang, Northeastern University, US; Weimin Fu, Xiaolong Guo, Kansas State University, US; Weidong Cao, George Washington University, US
- **BS-PDN-Last: Towards Optimal Power Delivery Network Design With Multifunctional Backside Metal Layers**
  Min Gyu Park, Amaan Rahman, Sung Kyu Lim, Georgia Institute of Technology, US
- **Towards Uncertainty-aware Robotic Perception via Mixed-signal BNN Engine Leveraging Probabilistic Quantum Tunneling**
  Likai Pei, Yu Zhou, Xingtian Wang, Xueji Zhao, Wanxin Huang, Boyang Cheng, Kai Ni, Mengxue Hou, Michael Niemier, Ningyuan Cao, University of Notre Dame, US; Halid Mulaosmanovic, Stefan Duenkel, Dominik Kleimaier, Sven Beyer, GlobalFoundries, DE
- **Dual-Issue Execution of Mixed Integer and Floating-Point Workloads on Energy-Efficient In-Order RISC-V Cores**
  Luca Colagrande, ETH Zürich, CH; Luca Benini, UniversitÃ di Bologna, IT
- **A High-Precision and Low-Cost Approximate Transform Accelerator for Video Coding**
  Zhijian Hao, Yue Hao, Xiaohua Ma, Xidian University, CN; Jiaming Liu, Chenlong He, Qi Zheng, Shushi Chen, Fudan University, CN; Jinchang Xu, Peking University, CN; Xiao Yan, Xi'an University of Posts & Telecommunications, CN

Session Chair(s): Ioannis Savidis, Drexel University; Kishor Kunal, NVIDIA

EVERYTHING ABOUT LLM AND TRANSFORMER ACCELERATORS

Time: 3:30 PM - 5:30 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session will provide an in-depth exploration of the latest advancements in accelerators designed for large language models (LLMs) and transformers. Attendees will gain insights into the intersection of hardware and AI, focusing on the innovations that enhance both computational efficiency and memory bandwidth with various quantization and prediction schemes. More specifically, the session covers the speculative and prediction on QKV computations, quantization schemes including block floating point and microscaling format, and how to sparsificate the models and leverage them. It also covers diffusion model acceleration and the intersection with compute-in-memory architecture.

- **3D-TokSIM: Stacking 3D Memory with Token-Stationary Compute-in-Memory for Speculative LLM Inference**
  Wentao Zhao, Meng Wu, Peiyu Chen, Yufei Ma, Tianyu Jia, Ru Huang, Le Ye, Peking University, CN; Boya Lv, Nanjing University, CN; Fengyun Yan, Nano Core Chip Electronic Technology, CN
- **A Memory-Efficient LLM Accelerator with Q-K Correlation Prediction using Cluster-Based Associative Array for Selective KV Accessing**
  Zikang Zhou, Kaiqi Chen, Xuyang Duan, Jun Han, Fudan University, CN
- **Precon: A Precision-Convertible Architecture for Accelerating Quantized Deep Learning Models across Various Domains Including LLMs**
  Jongwoo Park, Hyeonseong Kim, Jiyun Han, Seungkyu Choi, Kyung Hee University, KR
- **RADiT: Redundancy-Aware Diffusion Transformer Acceleration Leveraging Timestep Similarity**
  Youngjun Park, Sangyeon Kim, Yeonggeon Kim, Gisan Ji, Sungju Ryu, Sogang University, KR
- **SQ-DM: Accelerating Diffusion Models with Aggressive Quantization and Temporal Sparsity**
  Zichen Fan, Dennis Sylvester, University of Michigan, US; Steve Dai, Rangharajan Venkatesan, Brucek Khailany, Nvidia, US
- **XShift: FPGA-efficient Binarized LLM with Joint Quantization and Sparsification**
  Shuai Zhou, Huinan Tian, Sisi Meng, Jianli Chen, Jun Yu, Kun Wang, Fudan University, CN
- **BBAL: A Bidirectional Block Floating Point-Based Quantization Accelerator for Large Language Models**
  Xiaomeng Han, Jing Wang, Junyang Lu, Hui Wang, Ning Xu, Zhe Jiang, Southeast University, CN; Yuan Cheng, Nanjing University, CN; Xuanxi Zhang, Jilin Normal University, CN; Dawei Yang, Houmo, CN
- **An Algorithm-Hardware Co-design Based on Revised Microscaling Format Quantization for Accelerating Large Language Models**
  Yingbo Hao, Yi Zou, Yanfeng Yang, South China University of Technology, CN; Huangxu Chen, Hong Kong University of Science and Technology, CN

Session Chair(s): Yulhwa Kim, Sungkyunkwan University, KR

EXPLORING THE UNCHARTERED: FROM CHIPLETS TO ARCHITECTURE AND VALIDATION

Time: 3:30 PM - 5:30 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004,Level 3

Description: Welcome to the session "Explore the Uncharted," diving into pioneering research that pushes the boundaries of system exploration, design and validation. This session brings together innovative approaches for multi-FPGA routing and design space exploration leveraging machine learning and AI to tailor system-on-chip (SoC) parameters to specific workloads; or optimizing multi-chiplet systems, focusing on cache hierarchies and inter-chiplet networks. The session offers validation methods for 3D integrated systems using physics-based multi-faceted simulation, novel Gem5-based accelerator integration opportunities, as well as speeding up ISS simulations through optimized instruction decoders.

- **Gem5-AcceSys: Enabling System-Level Exploration of Standard Interconnects for Novel Accelerators**
  Qunyou Liu, David Atienza, École Polytechnique Fédérale de Lausanne, CH; Marina Zapater, HES-SO University of Applied Sciences and Arts Western Switzerland, CH
- **Adora Compiler: End-to-End Optimization for High-Efficiency Dataflow Acceleration and Task Pipelining on CGRAs**
  Jiahang Lou, State Key Laboratory of Integrated Chips and Systems, CN; Qilong Zhu, Yuan Dai, Zewei Zhong, Wenbo Yin, Lingli Wang, Fudan University, CN
- **Automated Generation of Decoders for Irregular Instruction Sets Using Information-Theoretic Decision Trees Construction Algorithms**
  Lillian Tadros, Technichal University of Dortmund, DE
- **Look Before You Leap: A Self-Review Bayesian Optimization Method for Constrained High-Dimensional Design Space Exploration**
  Xuyang Zhao, Yiyang Zhao, Zheng Wu, Zhaori Bi, Changhao Yan, Dian Zhou, Xuan Zeng, Fudan University, CN; Tianning Gao, The University of Texas at Dallas, US
- **High-Performance Computing Architecture Exploration with Stage-Enhanced Bayesian Optimization**
  Vincent Fu, Mohamed Benazouz, Lilia Zaourar, Université Paris-Saclay, FR; Alix Munier-Kordon, Sorbonne Université, FR
- **On Design Space Exploration of Cache System in Multi-Chiplet Systems**
  Yan Zhang, Xiaohang Wang, Zhejiang University, CN; Yingtao Jiang, University of Nevada, Las Vegas, US; Amit Singh, University of Essex, GB
- **From Flatland to Forest: Exploring Pareto-optimal Design through RTL Hierarchy Trees**
  Donger Luo, Xinheng Li, Hao Geng, ShanghaiTech University, CN; Qi Sun, Cheng Zhuo, Zhejiang University, CN; Bei Yu, The Chinese University of Hong Kong, HK
- **Synergistic Die-Level Router for Multi-FPGA System with Time-Division Multiplexing Optimization**
  Jiarui Wang, Yanjing Liu, Yibo Lin, Peking University, CN

Session Chair(s): Giuseppe Di Guglielmo, Fermilab; T V Narayanan, Ansys

FOLLOW THE LOGIC: ADVANCES IN LOGIC SYNTHESIS

Time: 3:30 PM - 5:30 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3006,Level 3

Description: Despite decades of prior research in logic synthesis and optimization, the field continues to be highly active and progress continues unabated, as evidenced by the eight exciting papers in this session. The first two papers leverage the concept of equivalence graphs (e-graphs) for functional verification and reducing structural bias prior to technology mapping. The next four papers contribute to more traditional logic synthesis thrusts, including Boolean decomposition, logic restructuring, refactoring, and challenges associated with structural bias of the subject graph. The last two papers present innovations in approximate logic synthesis, and synthesis of optimal logic circuits.

- **BoolE: Exact Symbolic Reasoning via Boolean Equality Saturation**
  Jiaqi Yin, Zhan Song, Chen Chen, Qihao Hu, Cunxi Yu, University of Maryland, College Park, US
- **E-morphic: Scalable Equality Saturation for Structural Exploration in Logic Synthesis**
  Chen Chen, Guangyu Hu, Yuzhe Ma, Hongce Zhang, Hong Kong University of Science and Technology, CN; Cunxi Yu, University of Maryland, College Park, US
- **EDGE: DBMS-Empowered Boolean Decomposition for GIG Synthesis**
  Ruofei Tang, Xinyi Zhang, Jianliang Xu, Hong Kong Baptist University, HK; Xuliang Zhu, Shanghai Jiao Tong University, CN; Lei Chen, Xing Li, Mingxuan Yuan, Huawei, HK
- **Logic Restructuring with Preserved Logic Blocks**
  Siang-Yun Lee, Heinz Riener, Sascha Richter, Cadence Design Systems, Inc., DE; Ankush Sood, Cadence Design Systems, Inc., US
- **ELF: Efficient Logic Synthesis by Pruning Redundancy in Refactoring**
  Dimitrios Tsaras, Zhiyao Xie, Hong Kong University of Science and Technology, HK; Xing Li, Lei Chen, Mingxuan Yuan, Huawei, HK

- **Mixed Structural Choice Operator: Enhancing Technology Mapping with Heterogeneous Representations**
  Zhang Hu, Yinshui Xia, Lunyao Wang, Zhufei Chu, Ningbo University, CN; Hongyang Pan, Fudan University, CN
- **Rank-Based Multi-Objective Approximate Logic Synthesis via Monte Carlo Tree Search**
  Yuyang Ye, Peng Xu, Tinghuan Chen Bei Yu, The Chinese University of Hong Kong, HK; Xiangfei Hu, Yuchen Liu, Southeast University, CN; Yu Gong, Nanjing University of Aeronautics and Astronautics, CN; Hao Yan, Longxing Shi, Southeast University, CN
- **Harrow: Synthesis of Optical Logic Circuits via Harmonic Mean and Integer Partition**
  Jun-Wei Liang, Iris Hui-Ru Jiang, Kai-Hsiang Chiu, National Taiwan University, TW

Session Chair(s): Giovanni De Micheli, EPFL; Eleonora Testa, Synopsys

PROGRAM, DEBUG, ACCELERATE: SOFTWARE INNOVATIONS

Time: 3:30 PM - 5:30 PM

Topic Area(s): Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: This session explores advances in sparse matrix computation, embedded AI, and system optimization. Topics include multimodal frameworks and tensor compilers that enhance sparse matrix operations, on-device training techniques that optimize neural network fine-tuning on constrained hardware, and AI-driven approaches for improving system security and reliability. Additionally, novel storage optimizations and efficient data processing methods will be presented. By integrating algorithmic innovations with hardware-aware strategies, these software innovations push the boundaries of performance, adaptability, and security in embedded computing.

- **SSpMV: A Sparsity-Aware SpMV Framework Empowered by Multimodal Machine Learning**
  Shengle Lin, Chubo Liu, Yan Ding, Kenli Li, Wangdong Yang, Hunan University, CN; Joey Zhou, Agency for Science, Technology and Research (A*STAR), SG
- **An Input-Aware Sparse Tensor Compiler Empowered by Vectorized Acceleration**
  Xianhao He, Haotian Wang, Jiapeng Zhang, Wangdong Yang, Kenli Li, Hunan University, CN; Anthony Chronopoulos, The University of Texas at San Antonio, US
- **Enabling On-Tiny-Device Model Personalization via Gradient Condensing and Alternant Partial Update**
  Zhenge Jia, Yiyang Shi, Zeyu Bao, Zirui Wang, Xin Pang, Huiguo Liu, Yu Duan, Zhaoyan Shen, Mengying Zhao, Shandong University, CN
- **Unlocking a New Rust Programming Experience: Fast and Slow Thinking with LLMs to Conquer Undefined Behaviors**
  Renshuang Jiang, Pan Dong, Zhenling Duan, Yu Shi, Xiaoxiang Fang, Yan Ding, Jun Ma, National University of Defense Technology, CN; Shuai Zhao, Sun Yat-sen University, CN; Zhe Jiang, Southeast University, CN
- **DroidFuzz: Proprietary Driver Fuzzing for Embedded Android Devices**
  Jianzhong Liu, Yuheng Shen, Yifei Chu, Yu Jiang, Tsinghua University, CN; Qiang Zhang, Wanli Chang, Hunan University, CN; Heyuan Shi, Central South University, CN
- **STREAM: Spatiotemporal Similarity-Based Efficient Approximate Median with Tunable Granularity**
  Fenfang Li, Huizhang Luo, Kenli Li, Chubo Liu, Hunan University, CN; Weichen Liu, Nanyang Technological University, SG; Anthony Chronopoulos, The University of Texas at San Antonio, US
- **Enabling Data-Deduplication-Assisted Data Relocation for Interlaced Magnetic Recording**
  Chen-Jui Tu, Shuo-Han Chen, National Yang Ming Chiao Tung University, TW
- **Location is Key: Leveraging LLM for Functional Bug Localization in Verilog Design**
  Bingkun Yao, Ning Wang, Nan Guan, City University of Hong Kong, HK; Jie Zhou, Xi Wang, Zhe Jiang, Southeast University, CN; Hong Gao, Zhejiang Normal University, CN

Session Chair(s): Hoeseok Yang, Santa Clara University; Younghyun Kim, Purdue University

STORAGE MEETS COMPUTING POWER FOR ADVANCING AI AND DATA PROCESSING EFFICIENCY

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3001, Level 3

Description: Compute-in-Memory (CIM) is emerging as a transformative approach for efficient AI acceleration, addressing challenges in data movement, energy efficiency, and computational bottlenecks. As deep learning evolves with diverse network topologies like GNNs and point-cloud models, CIM architectures and frameworks are being optimized for a wide range of use cases, from edge devices to data centers. This session explores novel CIM-based accelerators for tasks such as kNN search, graph neural networks, and point cloud neural networks, alongside hybrid CIM solutions for edge AI. It also covers optimization techniques for neural network models and presents a systematic framework for implementing and evaluating CIM platforms.

- **PICK: An SRAM-Based Processing-in-Memory Accelerator for K-Nearest-Neighbor Search in Point Clouds**
  Chen Nie, Zhezhi He, Shanghai Jiao Tong University, CN; Chao Jiang, Limin Xiao, Weifeng Zhang, Lenovo Research, CN

- **HH-PIM: Dynamic Optimization of Power and Performance with Heterogeneous-Hybrid PIM for Edge AI Devices**
  Sangmin Jeon, Kangju Lee, Kyeongwon Lee, Woojoo Lee, Chung-Ang University, KR
- **Anchor First, Accelerate Next: Revolutionizing GNNs with PIM by Harnessing Stationary Data**
  Jiaxian Chen, Yuxuan Qi, Yongbiao Zhu, Jianan Yuan, Kaoyi Sun, Tianyu Wang, Chenlin Ma, Yi Wang, Shenzhen University, CN
- **3D-SubG: A 3D Stacked Hybrid Processing Near/In-Memory Accelerator for Subgraph GNNs**
  Guoxiang Li, Runnan Xu, Ruohang Xu, Renati Tuerhong, Muhan Zhang, Le Ye, Yufei Ma, Peking University, CN; Yikan Qiu, Hangzhou Hikvision Digital Technology Co., Ltd., CN
- **PIMDup: An Optimized Deduplication Design on a Real Processing-in-Memory System**
  Chun-Le Yeh, Chien-Chung Ho, Da-Wei Chang, National Cheng Kung University, TW; Liang-Chi Chen, National Taiwan University, TW; Yu-Ming Chang, Wolley, TW
- **An Efficient Compute-in-Memory Based Accelerator for Point-Based Point Cloud Neural Networks**
  Xipeng Lin, Cong Wang, Shanshi Huang, Hongwu Jiang, The Hong Kong University of Science and Technology, CN
- **NDFT: Accelerating Density Functional Theory Calculations via Hardware/Software Co-Design on Near-Data Computing System**
  Buxin Tu, Qingcai Jiang, Xiaoyu Hao, Junshi Chen, Hong An, University of Science and Technology of China, CN
- **CIMFlow: An Integrated Framework for Systematic Design and Evaluation of Digital CIM Architectures**
  Yingjie Qi, Jianlei Yang, Yiou Wang, Yikun Wang, Dayu Wang, Ling Tang, Cenlin Duan, Xiaolin He, Weisheng Zhao, Beihang University, CN

Session Chair(s): Armin Roohi, University of Illinois, Chicago; Abhronil Sengupta, Pennsylvania State University

CHIPLET-BASED HETEROGENOUS INTEGRATION: PUSHING BEYOND MOORE'S LAW

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: As monolithic chips face technological and practical barriers, 2.5D/3D integration of predesigned chiplets is emerging as a key approach to continuously scale up processor performance, improve energy efficiency, enhance IP reuse at reduced cost, and expedite time-to-market. Such a paradigm shift requires a tight collaboration between packaging and chiplet designs throughout the entire design cycle, including technology, circuits, architectures and design automation tools. Designers must develop innovative 3D modules and chiplet interfaces, while evaluating physical and system-level tradeoffs in performance, data movement and energy efficiency. In addition, design and synthesis tools need to incorporate 3D integration and planning knowledge to enable seamless packaging and chiplet co-design. All these requirements pose substantial challenges to today's isolated ASIC and package design processes.

This special session features three visionary talks by industry and academic leaders, highlighting the essential research priorities for chiplet-packaging co-design. These talks delve into the technological foundations, state-of-the-art design methodologies for heterogeneous chiplets, emerging chiplet standards and IPs, and the pressing needs for simulation and design automation tools. Advances in this field will promote tight collaboration between chiplet and package designs, helping shed light on both the challenges and the vast potential of heterogeneous integration.

- **Advanced Package Design & System Co-Optimization for Heterogeneous Integration**
  Lalitha Immaneni, Intel, US
- **Advanced Packaging: Promise and the Needs**
  Ganesh Subbarayan, Purdue University, US
- **AMD InstinctTM MI300 Series Accelerator: Engineering Showcase of Heterogeneous Integration Technologies**
  Wonjun Jung, AMD, US
- **EDA for Heterogeneous Integration**
  Sachin S. Sapatnekar, University of Minnesota, US

Session Chair(s): Yu Cao, University of Minnesota

BUILDING SECURE CHIPS WITHOUT JEOPARDIZING DESIGN BUDGETS AND SCHEDULES

Time: 4:00 PM - 4:45 PM
Session Type: DAC Pavilion Panel
Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The importance of proactively securing semiconductor chips during the design phase has grown significantly over the past few years, driven by the rapidly increasing number of discovered chip security vulnerabilities, emerging industry standards, and new regulations and laws, among other factors. As a result, most would agree on the importance of a robust hardware security program and that security signoff should become another key checkbox before tape-out. Yet, translating this objective into reality is challenging due to tight tape-out schedules, lack of broad security knowledge, limited engineering resources, and the need for new cross-organizational coordination.

This panel of leading hardware security practitioners will discuss the various challenges of securing chips and share how to overcome them in practice, all while staying on schedule, within budget, and boosting competitiveness.

Moderator: Andreas Kuehlmann, Cycuity, US

Panelists: Rachana Maitra, Marvell, US; Mark Labatto, Booz Allen Hamilton, US; Vikram Khosa, ARM, US; Maurizio Paganini, Meta, US

INDUSTRY-LEADING 3D-IC MULTI-DIE SILICON COMPANIES DISCUSS THEIR MULTIPHYSICS CHALLENGES

Time: 4:15 PM - 5:15 PM
Session Type: Exhibitor Forum
Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Designers of multi-die 2.5D/3D-ICs have faced many new multiphysics issues that were not a concern for single-die design. These include thermal prototyping, electromagnetic coupling of digital signals, mechanical warpage of interposers, and more. This session is a moderated discussion that assembles a panel of experienced 3D-IC design engineers from leading silicon vendors to talk about their experiences with production projects. The adoption of multi-die technology is spreading to more design teams, and this is a valuable opportunity to understand what issues really matter, what lessons were learned, and which techniques that have been proven to work.

Moderator: Murat Becer, Ansys

Panelists: Sonia Leon, Intel; John Linford, Nvidia; Nitin Navale, AMD; Lluis Paris, TSMC

POSTER GLADIATOR BATTLE

Time: 5:00 PM - 6:00 PM
Session Type: Monday Poster Gladiator Battle
Room: DAC Pavilion, Level 2 Exhibit Hall

TUESDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 5:00 PM - 6:00 PM
Session Type: Engineering Poster
Room: Engineering Posters, Level 2 Exhibit Hall

1.1% DIE AREA REDUCTION IN CONSUMER AND INDUSTRIAL MCU-PRODUCTION SOC MEETING ANALOG ROUTING AND PERFORMANCE TARGETS

Abhishek Nigam, Ashutosh Chaubey, Jayapriya Arjunan, HCL Technologies Ltd., IN; Yusuke Tanabe, Juntaro Akashi, Seiichi Oshima, Toru Sugahara, Renesas Electronics Corporation, JP

18% DIE AREA REDUCTION IN UWB AUTOMOTIVE PRODUCTION SOC MEETING PERFORMANCE

Abhishek Nigam, Vinod Singh, Nilotpal Arjun, Swati Singh, Sateesh Potnuru, S Deepika, Bhanu Prakash, HCL Technologies Ltd., IN; Naoki Ueda, Masafumi Ieiri, Yusuke Okazaki, Renesas Electronics Corporation, JP

A COMPREHENSIVE ELECTROMAGNETIC ANALYSIS FLOW FOR DIE AND PACKAGE JOINT MODEL SIMULATION OF RF CHIPS DESIGN

Chaofan Zeng, Jie Hu, Xiaoming Si, Sanechips Technology Co., Ltd, CN; Yongsheng Guo, Ansys, CN

A ROBUST AND EFFICIENT VERIFICATION SUITE FOR AMS IP HDL MODELS FOR STREAMLINED SOC INTEGRATION

Rahul Kumar, Anil Dwivedi, Ankur Bal, Atul Bhargava, STMicroelectronics, IN

AACT: AUTOMATED ANALOG COVERAGE TOOL FOR MIXED SIGNAL VERIFICATION

Bhavya Shah, Aadhar Sharma, Gayathri M, Avinash Chaudhary, Atul Lele, Texas Instruments, IN

ACCELERATED ESD SIGN-OFF SOLUTION: AN EFFICIENT AND SCALABLE APPROACH

Smaritha Kasukurthi, Mathew Kaipanatu, Sainath Reddy Gummana, Google, IN; Sai Prabhakar Atluri, Ansys, US

ACCELERATING SEMICONDUCTOR TEST DATA ANALYSIS THROUGH CPU-GPU HYBRID COMPUTING: A RESOURCE OPTIMIZATION FRAMEWORK

Sanghyeok Park, Sungkyunkwan University, KR

ACCURATE MEMORY IR SIGN-OFF AT LOWER TECH NODES

Smaritha Kasukurthi, Mathew Kaipanatu, Akshay Gupta, Google, IN

TUESDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

ADVANCED STATE SPACE TUNNELING: DEBUG YOUR FORMAL COMPLEXITY USING WAVEFORMS!
Erik Seligman, Lars Lundgren, Mariane Goncalves, Gustavo Junquiera, Tulio Leao, Gabriela Bahia, Hakan Hjort, Craig Deaton, Cadence Design Systems, Inc., US; Varun Ramesh, Varun Ramesh, Tenstorrent, US

AI-BASED TRIMMING AND OPTIMIZATION FOR VOLTAGE REGULATORS: PROVEN ACCURACY WITH WAFER DATA
Doyoung Kim, Tei Cho, Eunsuk Park, Wonbeom Choi, Bonggil Kang, SK hynix, KR; Sungyoun Lee, Mohamed Atoua, Siemens, US

AI-ML MEETS SPICE TO ACHIEVE 6-SIGMA ACCURACY: A REVOLUTION IN STATISTICAL ANALYSIS
Aditya Vasisth, Rajesh Narwal, Pravesh Saini, ST Microelectronics, IN; Prayes Jain, Cadence Design Systems, Inc., IN

AN EFFICIENT HIERARCHICAL CHIP-TOP LEVEL EMIR SIGNOFF METHODOLOGY FOR LARGE AUTOMOTIVE SOCS.
Akhilesh Mishra, Abhinav Gaur, NXP, IN; Ramesh Sharma, Shreyashi, Ansys, IN

APPROACH FOR QUALITY DV USING C2RTL FOR ALGORITHMIC DESIGNS AUTHORS: NEEMA AGARWAL, HIMANSHU CHAUHAN, HARSH SETIA, ATHARVA MAHESH KAKDE, KETKI GOSAVI
Neema Agarwal, Himanshu Chauhan, Harsh Setia, Samsung Semiconductor, IN; Atharva Kakde, Ketki Gosavi, Cadence Design Systems, Inc., IN

AUDIT FLOW: A FAST QUALITY CHECKER TOOL FOR EARLY DESIGN CONVERGENCE
Manjunath Nayak, Subhash Uppala, Anoop Singh, Ayan Datta, Western Digital, IN

AUTOLNKGEN: AUTOMATED RANDOM LINKER FILE GENERATION FRAMEWORK FOR HETEROGENOUS SOC VERIFICATION & VALIDATION
Mohan Udayakumar, Yogeshwaran Shanmugam, Suraj Salian, Rakesh YC, Aswin B, Texas Instruments, IN

AUTOMATED - BUS ROUTING SOLUTION FOR EFFICIENT DRC CLEAN TESTCHIP DESIGN
Manvi Dhawan, Atul Bhargava, Rajeev Singh, Anil Dwivedi, Ankur Bal, STMicroelectronics, IN; Akshita Bansal, Fabien Campana, Laurent Saint-Marcel, Cadence Design Systems, Inc., FR

AUTOMATED QA FOR STANDARD CELL LIBRARIES USED IN RAIN RFID CHIPS
Keven Dunn, Lee Burns, Impinj, US; Cooper Robertson, Siemens, CA

AUTOMATED TOPOLOGY BASED PIN ACCESS CHECKER FOR CORRECT BY CONSTRUCTION STANDARD CELLS DESIGN
Sharmistha Sinha, Anuradha Ray, Anand Mishra, Frederic Avellaneda, Atul Bhargava, Ankur Bal, Anil Dwivedi, STMicroelectronics, IN; Akshita Bansal, Hitesh Marwah, Arvind Kumar, Neha Agrawal, Vishesh Kumar, Cadence Design Systems, Inc., IN

BALANCING PERFORMANCE AND SIDE-CHANNEL RESILIENCE IN A LIGHTWEIGHT ECC CRYPTOSYSTEM
Harikrishnan Balagopal, Lang Lin, Norman Chang, Ansys, US; Mitra Mirhassani, Seyedeh Nejati, University of Windsor, CA

CHIP RELIABILITY WITH ANTENNA DISCHARGE PATH CONSIDERATION
Heng Lan Lau, John Ferguson, Siemens, US

CTS WITH MACHINE LEARNING NDR
Sungsu Byun, Samsung, KR

DESIGN QUALITY IMPROVEMENT THROUGH AUTOMATION
Sagar Jogur, Mangesh Dhantole, Texas Instruments, IN

DETECTION OF FUNCTIONAL AND CURRENT RELATED BUGS IN SOC THROUGH FULL CHIP SPICE SIMULATIONS (FCS)
Manmohan Rana, Nishant Kaundal, STMicroelectronics, IN; Rakesh Shenoy, Synopsys, IN

DIGITAL FILTER ARCHITECTURE FOR ROBUST TRACKING OF ON-CHIP LOW FREQUENCY OSCILLATOR PERIOD, ENABLING CRYSTAL LESS BLE OPERATION IN LOW POWER WIRELESS MCUS
Anurag Choudhury, Ashutosh Mishra, Texas Instruments, IN; Robin Hoel, Torjus Kallerud, Texas Instruments, NO

EFFECTIVE WAYS OF ANALYZING AND OPTIMIZING VOLTAGE VARIATION CHALLENGES FOR 3DIC CHIPS
Mingyang Liu, Runjian Wang, Hengzhi Hu, Minglu Xu, Yue Heng, Hangzhou Zhicun (Witmem) Technology Co., Ltd., CN; Ran Zhang, Shuoyue Cui, Xiaomei You, Ansys, CN; Long Kong, Witmem, CN

EFFICIENT HARDWARE FUZZING BASED ON SYSTEMC
Byunghoon Lee, Jaewoo Im, Samsung, KR; Ki-Whan Song, Samsung, KR; Jiyuan Wang, Ben Limpanukorn, Miryung Kim, University of California, Los Angeles, US

EFFICIENT TRANSLATION OF OPENACCESS DESIGN DATA TO THE OASIS FORMAT
Robert Allen, Mitch DeHond, Ron Rose, Margaret Allen, Matt Guzowski, Nayo Ogilvie, IBM, US

ENERGY EFFICIENT I3C IP SUBSYSTEM FOR LOW POWER IOT
Aradhana Kumari, STMicroelectronics, FR

ENHANCING VERIFICATION EFFICIENCY WITH GARBAGE-MODEL METHODOLOGY
Smadar Eliyahu-Shulemzon, Stas Yosupov, Xsight Labs, IS

TUESDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

ENZO: COMPREHENSIVE DFT METHODOLOGY FOR MCU CLASS OF DEVICES
Arshdeep Singh, Jahnavi Pragada, Vishal Diwan, Texas Instrument, IN

FORMAL MEETS SIMULATION: ACCELERATE VERIFICATION CLOSURE USING MULTIPLATFORM TECHNOLOGIES
Anunay Bajaj, Amrita Patil, Kirti Srivastava, Cadence Design Systems, Inc., IN

GUIDED PHYSICAL POWER OPTIMIZATION OF AI SILICON
Aditya Chandrasekar Ramachandran, Microsoft, US

HIGH FIGURE OF MERIT POLYPHASE DECIMATION CORE IP
Ankur Bal, Anupam Jain, Atul Bhargava, Anil Dwivedi, STMicroelectronics, IN

IC FOLDING FOR ENHANCED PERFORMANCE IN HOMOGENEOUS RF-AMS SYSTEMS
Parv Malhotra, Neha Agrawal, Hitesh Marwah, Mike Lin, Praveen Pillai, Cadence Design Systems, Inc., US; Arnold Ginetti, Cadence Design Systems, Inc., FR; Jignesh Patel, GlobalFoundries, US; Aditya Ramesha, GlobalFoundries, IN

INNOVATIVE RDL PEX FLOW WITH CALIBRE, ENHANCES DESIGN RELIABILITY AND PERFORMANCE
Siemens, EG

JANUS - TWIN-FACED DEBUGGING - ANECDOTES FROM FORMAL, SECURITY & TIMING EXCEPTION VERIFICATION
Srinivasan Venkataramanan, VerifWorks, GB; Ajeetha Kumari Venkatesan, AsFigo Technologies, GB; Hemamalini Sundaram, Verifworks, IN

MAXIMIZING IR SIGN-OFF COVERAGE USING SIGMA-AV AND ITS BENEFIT ON PPA
Sandeep Gajbhare, Mathew Kaipanatu, Google, IN

NETLIST POWERED EMULATION PARADIGM: PIONEERING BREAKTHROUGHS IN GATE LEVEL VERIFICATION
Samhith Pottem, Vasudeva Reddy, Sarang Kalbande, Garima Srivastava, Samsung Semiconductor, IN; Jaesung Park, Hyundon Kim, Samsung, KR

NOVEL SHIFT-LEFT METHODOLOGY FOR SYSTEM POWER INTEGRITY ANALYSIS WITH EARLY CHIP POWER MODEL
Lyubomir Kerachev, Olivier Bayet, STMicroelectronics, FR; Ravi Thiruveedhula, Ansys, US

PATTERN-BASED ABSTRACTION FOR MIXED TRANSISTOR-LEVEL STATIC TIMING ANALYSIS
Xin Zhao, Robert Allen, Kerim Kalafala, IBM, US

PEAK POWER OPTIMIZATION IN RTL2GDS FLOW USING GUIDANCE FROM RTL POWER OPTIMIZATION TOOLS
Sanchita Gupta, Manish Kumar, Vijay Tayal, Amit Dey, Siemens, IN; Ouidiane Chafik, Kamal Ait-chergui, Youssef Saroukh, Soufian Bouazizi, Siemens, MA; Faheem Ahmed Qazi, Siemens, US

PHYSICAL AWARE RAM SEQUENTIAL ATPG FOR IR PREVENTION
Chen Yuan Kao, Global Unichip Corp., TW; Jerry Chen, Global Unichip Corp., US

PHYSICAL DESIGN INDEPENDENT-IR SOLVER FOR EARLY FIRST CUT SOC PG ANALYSIS
Prateek Pendyala, Google, TW; Jingwei Zhang, T Govindaswamy Rahul Sai, Google, US

PORTFOLIO RE-CHARACTERIZATION USING AI
Ray Valencia, Siemens, CA; Ajay Kumar, Siemens, GB; Reshma Krishnakumar, Swanand Kulkarni, Abhishek Sharma, NXP, IN

POWER-AWARE DFT-DRIVEN HIGH CONFIDENCE EMIR SIGNOFF FOR LOW POWER AUTOMOTIVE SOCS
Shining Dong, Glen Ge, NXP Semiconductors, CN; Rong Wang, Shuoyue Cui, Chang Zhao, Ansys, CN

RECIPE EXPLORER: CRAFTING THE MISSING PD FLOW LAYER
Aditya Chandrasekar Ramachandran, Microsoft, US

RECONFIGURABLE VECTOR FLOATING POINT ACCELERATOR ON FPGAS
Himanshu Rai, Sasi Snigdha Yadavalli, International Institute of Information Technology Bangalore, IN; Aishwarya Sridhar, Infineon Technologies Semiconductors, IN; Nanditha Rao, IBM, IN

REFRESH YOUR UVM TESTBENCH WITH A SPRITZ OF PYTHON
Matthew Ballance, AMD, US

SCALABLE DEBUGGING FOR DATA CENTERS: ENSURING RELIABILITY FROM DESIGN TO OPERATIONS
Suresh Duthiraru, Sandesh Putturaya, Microsoft, US; Rolf Kuehnis, Lauterbach, US; Matthias Zens, Lauterbach, DE

SIMULATION-AWARE GATE RESISTANCE MODELING BEFORE POST-LAYOUT SIMULATION
Hsiu-Chuang Chang, Hsiang-Ho Chang, Ke-Ying Su, TSMC, TW

SIMULATION-BASED PRE-SILICON SIDE-CHANNEL ANALYSIS OF AES-GCM
Emrah Karagoz, Ferhat Yaman, Amitabh Das, Sourabh Goyal, Advanced Micro Devices (AMD), US; Karthik Gedela, Advanced Micro Devices (AMD), IN

SOFT ERROR SIMULATION TOOLS, FROM 45NM TO 3NM
JC Bouzigues, IROC Technologies, US; Maximilien Glorieux, Issam Nofal, IROC Technologies, FR

THE EVOLUTION OF COLLABORATIVE OPEN SOURCE HARDWARE DEVELOPMENT
Robert Mains, Chips Alliance, US; Michael Gielda, Antmicro, PL; Tom Spyrou, Precision Innovation, US; Prabhu Jayanna, Advanced Micro Devices (AMD), US; Bryan Kelly, Microsoft, US; Andres Lagar-Cavilla, Google, US; Paul Chou, Nvidia, US

THE FUTURE OF MOBILITY
Steve Greenfield, Automotive Ventures, US

TUESDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

TIMING VISUALIZER AI ASSISTANT: A NOVEL MACHINE LEARNING APPLICATION FOR EFFICIENT TIMING TRIAGE

Santanu Das, Nidhi Gupta, Chakradhar Thallapaka, Haritha Mudimela, Prabhat Maurya, Aryan Garg, Indramani Yadav, Sachin Gupta, Gireesh kumar K M, IBM, IN; Kerim Kalafala, Charles Gates, Hemlata Gupta, IBM, US

USB4 MAC VERIFICATION: OVERCOMING SERIAL INTERFACE AND SIMULATION TIME CHALLENGES

Nehal Patel, Nirav Toliya, Cadence Design Systems, Inc., IN

DEMOCRATIZE CHIP DESIGN – WITH DEEP LEARNING AND AUTOMATED CODE TRANSFORMATION

Time: 8:45 AM - 10:00 AM

Topic Area(s): AI, Design

Session Type: Keynote

Room: 3007, Level 3

Description: In the past six decades, electronic design automation (EDA) has done a remarkable job to improve the productivity of hardware designers. I would like to argue that the next phase of EDA is to enable many software programmers to design their own chips or accelerators for a wide range of applications for better performance and energy efficiency, which is much needed as we are approaching the end of Moore's Law scaling. In this talk, I shall present our effort towards this goal. Coupled with our multi-decade research high-level synthesis (HLS), we developed and integrated multiple deep learning techniques, such as graph neural networks (GNNs) and large language models (LLMs), cross-modality learning, active learning with cross-entropy minimization, hierarchical mixture of expert modeling, and agent-based design space exploration. For regular structures, such as systolic arrays, stencil computation, or even more general affine programs used almost all deep learning kernel, we can also use mathematical programming to achieve automated code transformation. Combining these techniques, we show very promising results of mapping software code to high-quality silicon implementations.

Speaker: Jason Cong, University of California, Los Angeles

THE FUTURE OF MOBILITY

Time: 10:15 AM - 11:00 AM

Session Type: Analyst Presentation

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: The way we transport humans and cargo is evolving at a pace not experienced since the beginning of the industrial revolution.

This session will provide a glimpse into the future of mobility, including grand transportation, marine, aviation and space.

We'll not only discuss vehicle autonomy, electrification and connectivity, but explore how new technologies are impacting other modes of transportation.

Speaker: Steve Greenfield, Automotive Ventures, US

GENAI-POWERED CYBER-RESILIENT RTL FOR SECURE AND ROBUST SEMICONDUCTOR DEVICES

Time: 10:30 AM - 11:00 AM

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Semiconductor devices face increasing risks of attacks, exploits, and cyber vulnerabilities. Complex supply chains, distribution channels, and in-field deployments make it difficult to secure a device at every point in its lifespan. This session will focus on a new technique that hardens semiconductor designs to thwart malicious actors from embedding Trojans, introducing design flaws, or implementing manufacturing changes that compromise device functionality, reliability, or data integrity.

We will share a patented design hardening approach that not only supports thorough validation but also enables quantitative assessment of security improvements at RTL level. Central to this approach is intelligent instrumentation, based on a sophisticated method that precisely identifies and characterizes chip vulnerabilities, assesses their severity and impact, and strategically implements countermeasures. Our method leverages supervised machine learning to make data-driven tradeoff between security efficacy and cost ensuring optimal design instrumentation.

Attendees will gain insight into advanced GenAI and ML-based design for security and trust methodology that takes a proactive approach to microelectronics security at the RTL level. The session will detail how semiconductor devices can be made secure - monitored for anomalous behavior - from design to fabrication to deployment.

Speaker: Peter Levin, Amida Technology Solutions, US

IP GOLD – NEW DIGITAL DESIGN NUGGETS

Time: 10:30 AM - 12:00 PM

Topic Area: IP

Session Type: Engineering Track

Room: 2010, Level 2

Description: This session presents six interesting digital IP components and design techniques. It covers resilience against side channel attacks in encryption IP as well as new blocks addressing the need for communication protocols, low power clocks, decimation cores and vector floating point math units.

- **Balancing Performance and Side-Channel Resilience in a Lightweight ECC Cryptosystem**
  Harikrishnan Balagopal, Lang Lin, Norman Chang, Ansys, US; Mitra Mirhassani, Seyedeh Nejati, University of Windsor, CA

- **Simulation-Based Pre-Silicon Side-Channel Analysis of AES-GCM**
  Emrah Karagoz, Karthik Gedela, Ferhat Yaman, Amitabh Das, Sourabh Goyal, Advanced Micro Devices (AMD), US
- **Energy Efficient I3C IP Subsystem for Low Power IoT**
  Aradhana Kumari, STMicroelectronics, FR
- **Hybrid and Adaptive Digital Filter Architecture for Robust Tracking of On-Chip Low Frequency Oscillator Period, Enabling Crystal Less BLE Operation in Low Power Wireless MCUs**
  Anurag Choudhury, Ashutosh Mishra, Texas Instruments, IN; Robin Hoel, Torjus Kallerud, Texas Instruments, NO
- **High Figure of Merit Polyphase Decimation Core IP**
  Ankur Bal, Anupam Jain, Atul Bhargava, Anil Dwivedi, STMicroelectronics, IN
- **Reconfigurable Vector Floating Point Accelerator on FPGAs**
  Himanshu Rai, Sasi Snigdha Yadavalli, International Institute of Information Technology, Bangalore, IN; Aishwarya Sridhar, Infineon Technologies, IN; Nanditha Rao, IBM, IN

Session Chair(s): Bhaskar Vedula, Intel, Portland/OR, US

THE EVOLUTION OF COLLABORATIVE OPEN SOURCE HARDWARE DEVELOPMENT

Time: 10:30 AM - 12:00 PM

Topic Area: Systems and Software

Session Type: Engineering Track

Room: 2010, Level 2

Description: With the evolution and establishment of open source software, open hardware is aspiring to a similar stature of dependability and reliability in the industry. Over the past years, the chip design industry has witnessed the growth of open source and collaborative efforts across the entire spectrum of hardware development. The community of open hardware comprises several key ingredients necessary to design and build a chip, and those ingredients are served to a chip designer via a design environment.

These include:

- Hardware instruction sets such as RISC-V, OpenPower
- Process Design Kits (PDKs) representing the manufacturing ingredients to design a chip
- Electronic Design Automation (EDA) software used for the construction, functional, electrical, and design verification of the design
- Cloud based design enablement platform
- Collaborative design of SoC components using a mix of new and off the shelf open source IP

This session will provide the audience with the latest developments in open source PDKs, EDA, cloud based design environments, and a collaborative chip design project known as Caliptra.

Organizer(s): Robert Mains, Chips Alliance, US

Moderator: Robert Mains, Chips Alliance, US

Speakers: Michael Gielda, Antmicro, PO; Tom Spyrou, Precision Innovation, US; John Traver, Advanced Micro Devices (AMD)

VERIFICATION INNOVATION: SHAPING THE FUTURE OF DESIGN VALIDATION

Time: 10:30 AM - 12:00 PM

Session Type: Engineering Track

Room: 2008, Level 2

Description: Join us to learn about new strategies in the catch-up game verification engineers play daily with the increasing design complexity and tighter schedules. In this session, presenters will talk about advanced verification techniques spanning from RTL to GLS covering Python, UVM and SystemC driven solutions.

- **Refresh Your UVM Testbench with a Spritz of Python**
  Matthew Balance, Advanced Micro Devices (AMD), US
- **AACT: Automated Analog Coverage Tool for Mixed Signal Verification**
  Bhavya Shah, Aadhar Sharma, Gayathri M, Avinash Chaudhary, Atul Lele, Texas Instruments, IN
- **AUTOLNKGEN: Automated Random Linker File Generation Framework for Heterogenous SoC Verification & Validation**
  Mohan Udayakumar, Yogeshwaran Shanmugam, Suraj Salian, Rakesh YC, Aswin B, Texas Instruments, IN
- **Efficient Hardware Fuzzing Based on SystemC**
  Byunghoon Lee, Jaewoo Im, Ki-Whan Song, Samsung, KR; Jiyuan Wang, Ben Limpanukorn, Miryung Kim, University of California, Los Angeles, CA
- **Netlist Powered Emulation Paradigm: Pioneering Breakthroughs in Gate Level Verification**
  Samhith Pottem, Vasudeva Reddy, Garima Srivastava, Samsung Semiconductor, IN; Jaesung Park, Sarang Kalbande, Hyundon Kim Samsung, KR
- **Enhancing Verification Efficiency with Garbage-Model Methodology**
  Smadar Eliyahu-Shulemzon, Stas Yosupov, Xsight Labs, IS

Session Chair(s): Dave Rich, Siemens, US

ML-POWERED LOGIC SYNTHESIS

Time: 10:30 AM - 12:00 PM

Topic Area: EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: The use of machine learning (ML) in EDA is a burgeoning research direction and this session includes six papers aligned with this important theme. The first three papers make use of large language models (LLMs) for generating synthesis scripts and for generating Chisel and Verilog RTL code. The next paper uses generative AI, a diffusion model, for logic optimization. The next paper is related to multiplexer synthesis, and offers a significant area reduction vs. the state-of-the-art. The last paper uses an actor-critic neural-network approach in the context of optimizing dynamic voltage-frequency scaling (DVFS).

- **ChatLS: Multimodal Retrieval-Augmented Generation and Chain-of-Thought for Logic Synthesis Script Customization**
  Haisheng Zheng, Shanghai AI Laboratory, CN; Haoyuan Wu, Zhuolun He, The Chinese University of Hong Kong, HK
- **MAGE: A Multi-Agent Engine for Automated RTL Code Generation**
  Yujie Zhao, Hejia Zhang, Hanxian Huang, Jishen Zhao, University of California, San Diego, US
- **ReChisel: Effective Automatic Chisel Code Generation by LLM with Reflection**
  Juxin Niu, Nan Guan, City University of Hong Kong, HK; Xiangfeng Liu, Northeastern University, CN; Dan Niu, Xi Wang, Zhe Jiang, Southeast University, CN
- **Efficient Continuous Logic Optimization with Diffusion Model**
  Yikang Ouyang, XiaoFei Yu, Jiadong Zhu, Yuzhe Ma, The Hong Kong University of Science and Technology, CN; Tinghuan Chen, The Chinese University of Hong Kong, Shenzhen, CN
- **smaRTLy: RTL Optimization with Logic Inferencing and Structural Rebuilding**
  Chengxi Li, Yang Sun, Evangeline Young, The Chinese University of Hong Kong, HK; Lei Chen, Yiwen Wang, Mingxuan Yuan, Huawei, HK
- **Centralized Training and Decentralized Control Through the Actor-Critic Paradigm for Highly Optimized Multicores**
  Benedikt Dietrich, Heba Khdr, Joerg Henkel, Karlsruhe Institute of Technology, DE

Session Chair(s): Peipei Zhou, Brown University; Cunxi Yu, University of Maryland

SMART CIRCUITS, SMARTER ALGORITHMS: AI-DRIVEN INNOVATIONS IN CIRCUIT MODELING AND OPTIMIZATION

Time: 10:30 AM - 12:00 PM

Topic Area: AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session delves into the application of machine learning across different stages of hardware design, from analog circuits, sequential circuits, physical design, and simulation. The first set of presentations focuses on leveraging AI for optimizing analog circuit design, with talks exploring innovations in parasitic capacitance prediction for AMS circuits. The third presentation shifts focus to sequential circuit design, introducing novel methods for behavior-centric optimization through machine learning techniques. Next, a physical design recipe recommender is presented, showcasing how AI can enhance the design process. Finally, the session concludes with two talks on simulation, examining the integration of machine learning with SPICE models and the use of neural compact modeling for accelerating design-technology co-development.

- **Few-Shot Learning on AMS Circuits and Its Application to Parasitic Capacitance Prediction**
  Shan Shen, Yibin Zhang, Hector Rodriguez, Wenjian Yu, Tsinghua University, CN
- **Decoupling Analog Circuit Representation from Technology for Behavior-Centric Optimization**
  Jintao Li, Jiang Xiao, Yun Li, University of Electronic Science and Technology of China, CN; Haochang Zhi, Southeast University, CN; Keren Zhu, Fudan University, CN
- **MOSS: Multi-Modal Representation Learning on Sequential Circuits**
  Mingjun Wang, Bin Sun, Jianan Mu, Feng Gu, Xinyu Zhang, Silin Liu, Gao Jun, Zizhen Liu, Shengwen Liang, Jing Ye, Xiaowei Li, Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN; Boyu Han, Stanford University, US; Tianmeng Yang, Peking University, CN; Yihan Wen, Husheng Han, Beijing University of Technology, CN; Hui Wang, CASTEST, CN; Bei Yu, The Chinese University of Hong Kong, HK
- **InsightAlign: A Transferable Physical Design Recipe Recommender Based on Design Insights**
  Hao-Hsiang Hsiao, Georgia Institute of Technology, US; Sudipto Kundu, Wei Zeng, Wei-Ting Chan, Deyuan Guo, Synopsys, US; Sung Kyu Lim, Georgia Institute of Technology, US

- **Self-Attention To Operator Learning-Based 3D-IC Thermal Simulation**
  Zhen Huang, Hong Wang, Yu Zhang, University of Science and Technology of China, CN; Wenkai Yang, ShanghaiTech University, CN; Muxi Tang, Tsinghua University, CN; Depeng Xie, BTD Technology, Inc, CN; Ting-Jung Lin, Lei He, Eastern Institute of Technology, CN; Wei Xing, The University of Sheffield, GB
- **Accelerating Design-Technology Co-Development Using Neural Compact Modeling and Data-Driven SPICE Simulation**
  Yongjeong Lee, Seungsoo Lee, Jeongyeol Kim, Jungyun Choi, Samsung, KR; Zhaojie Li, Dehuang Wu, Synopsys, CN; Joddy Wang, Synopsys, US

Session Chair(s): Jun Shiomi, Osaka University; Subhajit Dutta Chowdhury, Advanced Micro Devices (AMD)

SMARTER COMPUTE, FASTER INFERENCE: OPTIMIZING AI SYSTEMS ON EDGE

Time: 10:30 AM - 12:00 PM

Topic Area: AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: As AI continues to push toward real-time and resource-efficient processing, optimizing both compute and memory across diverse hardware platforms becomes crucial. This session introduces techniques that aim to improve AI efficiency at the edge, including federated learning frameworks that account for real-world constraints, proactive strategies for mitigating inference cold starts, and novel data streaming techniques that decouple memory access. Additionally, new approaches in cross-layer simulation, task-oriented detection, and low-latency graph processing on FPGAs showcase how hardware-software co-design can unlock smarter, faster, and more efficient AI systems.

- **PracMHBench: Re-Evaluating Model-Heterogeneous Federated Learning Based on Practical Edge Device Constraints**
  Yuanchun Guo, Bingyan Liu, Yulong Sha, Zhensheng Xian, Beijing University of Posts and Telecommunications, CN
- **SimPhony: A Device-Circuit-Architecture Cross-Layer Modeling and Simulation Framework for Heterogeneous Electronic-Photonic AI System**
  Ziang Yin, Jeff Zhang, Jiaqi Gu, Arizona State University, US; Meng Zhang, Amir Begovic, Zhaoran Huang, Rensselaer Polytechnic Institute, US
- **DataMaestro: A Versatile and Efficient Data Streaming Engine Bringing Decoupled Memory Access To Dataflow Accelerators**
  Xiaoling Yi, Yunhao Deng, Ryan Antonio, Fanchen Kong, Marian Verhelst, KU Leuven, BE; Guilherme Paim, INESC-ID, University of Lisbon, PT
- **iTaskSense: Task-Oriented Object Detection in Resource-Constrained Environments**
  SungHeon Jeong, Hamza Errahmouni Barkam, Hyunwoo Oh, Hanning Chen, Tamoghno Das, Zhen Ye, Mohsen Imani, University of California, Irvine, US
- **PaSK: Cold Start Mitigation for Inference with Proactive and Selective Kernel Loading on GPUs**
  Xuanteng Huang, Jiangsu Du, Nong Xiao, Xianwei Zhang, Sun Yat-sen University, CN
- **FLAG: An FPGA-Based System for Low-Latency GNN Inference Service Using Vector Quantization**
  Yunki Han, Taehwan Kim, Jiwan Kim, Seohye Ha, Lee-Sup Kim, Korea Advanced Institute of Science and Technology (KAIST), KR

Session Chair(s): Xiaoxuan Yang, University of Virginia; Shihao Song, Nvidia

SQUEEZING PLACEMENT FROM FPGAS, MACROS, DOWN TO THE CELL LEVEL

Time: 10:30 AM - 12:00 PM

Topic Area: EDA

Session Type: Research Manuscript

Room: 3006, Level 3

Description: From block level to the transistor level, this session has placement for everyone. Learn about DSP placement for FPGA-based CNN acceleration, large scale macro placement, unified placement and routing, improved congestion modeling, and constructing the latest CFET standard cell libraries. Join us to explore the many facets of placement to optimize advanced-node semiconductor design.

- **DSPlacer: DSP Placement for FPGA-Based CNN Accelerator**
  Baohui Xie, Xinrui Zhu, Zhiyuan Lu, Yuan Pu, Tongkai Wu, Bei Yu, Tinghuan Chen, The Chinese University of Hong Kong, CN; Xiaofeng Zou, National University of Defense Technology, CN
- **ReMaP: Macro Placement by Recursively Prototyping and Periphery-Guided Relocating**
  Yunqi Shi, Xi Lin, Ke Xue, Chao Qian, Zhi-Hua Zhou, Nanjing University, CN; Siyuan Xu, Shixiong Kai, Mingxuan Yuan, Huawei, HK
- **RUPlace: Optimizing Routability via Unified Placement and Routing Formulation**
  Yifan Chen, Jing Mai, Zuodong Zhang, Yibo Lin, Peking University, CN
- **Differentiable Net-Moving and Local Congestion Mitigation for Routability-Driven Global Placement**
  Wenchao Li, Hongxi Wu, Wenxing Zhu, Fuzhou University, CN; Duanxiang Liu, Shanghai UniVista Industrial Software Group Co., Ltd., CN; Xingquan Li, Peng Cheng Laboratory, CN

- **Comprehensive Placement and Routing Framework with Guaranteed In-Cell Routability for Synthesizing Complementary-FET Cells**
  Zhengzhe Zheng, Yinuo Wu, Keyu Peng, Chao Wang, Ziran Zhu, Southeast University, CN
- **Synthesis of CFET Cell Library Leveraging Backside Metal Routing**
  Ting-Xin Lin, Yih-Lang Li, National Yang Ming Chiao Tung University, TW

Session Chair(s): Xiaoxuan Yang, University of Virginia, Stanford University; Shihao Song, Nvidia

TO ABSTRACT OR NOT TO ABSTRACT THE STORAGE LAYER

Time: 10:30 AM - 12:00 PM

Topic Area: Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: While several studies seek to transparently optimize the storage devices by keeping a strong abstraction thus relieving application designers, others tend to give more control to take full advantage of the high performance promised by flash memory technology, thus breaking the traditional abstraction layer at the cost of more complexity. This session explores novel designs on both sides of abstraction level for novel technologies such as zoned namespace devices, computational storage, and Shingled magnetic recording.

- **SuperCopyback: Revisiting Copyback on Modern High-Performance NAND Flash-based SSDs**
  Dong Huang, Bo Ding, Wei Tong, Dan Feng, Huazhong University of Science and Technology, CN
- **The Unwritten Contract of Cloud-Based Elastic Solid-State Drives**
  Yingjia Wang, Ming-Chang Yang, The Chinese University of Hong Kong, HK
- **MiniWear: Minimizing Flash Wear via Hybrid Persistent Cache for Extended EF-SMR Lifetime**
  Chenlin Ma, Kaoyi Sun, Yuxuan Qi, Jiaxian Chen, Xiaochuan Zheng, Tianyu Wang, Yi Wang, Shenzhen University, CN
- **Leopard: Hardware Pass-Through Remote Storage Access with Queue Concurrency for Edge Intelligent Workstations**
  Wenjie Wang, Bo Peng, Jianguo Yao, Haibing Guan, Shanghai Jiao Tong University, CN
- **FineRR-ZNS: Enabling Fine-Granularity Read Refreshing for ZNS SSDs**
  Jun Li, Xiaobai Chen, Jieming Yin, Nanjing University of Posts and Telecommunications, CN; Zhibing Sha, Yang Fan, Jianwei Liao, Southwest University of China, CN; Xiaofei Xu, RMIT University, AU
- **StreamCSD: Host-Transparent SSD Stream Management via In-Storage Content Learning**
  Wenjie Li, Yelin Shan, Jiapin Wang, Yunxin Huang, Yafei Yang, Tao Lu, DapuStor Corporation, CN; Xiang Chen, You Zhou, Fei Wu, Huazhong University of Science and Technology, CN

Session Chair(s): Nima TaheriNejad, Heidelberg University

TRUSTED AI ACCELERATION: SECURE ARCHITECTURES, PRIVACY, AND RESILIENCE IN ML HARDWARE

Time: 10:30 AM - 12:00 PM

Topic Area: Security

Session Type: Research Manuscript

Room: 3002, Level 3

Description: As AI accelerators become increasingly integral to modern computing, ensuring their security and privacy is paramount. This session explores the key challenges in this domain, focusing on side-channel vulnerabilities, privacy-preserving computation techniques, and the design of secure deep learning hardware architectures. Topics include power-based attacks on XGBoost accelerators, efficient zero-knowledge proofs for verifiable computing, and fully homomorphic encryption (FHE) acceleration for client-side privacy. Additionally, the session covers secure DNN accelerators leveraging hardware/software co-design and lightweight reconfigurable computing to protect AI intellectual property.

- **Power-Based Side-Channel Attack on XGBoost Accelerator**
  Yimeng Xiao, Aydin Aysu, Paul Franzon, North Carolina State University, US; Archit Gajjar, Hewlett Packard Enterprise, US
- **zkVC: Fast Zero-Knowledge Proof for Private and Verifiable Computing**
  Yancheng Zhang, Mengxin Zheng, Yan Solihin, Qian Lou, University of Central Florida, US; Xun Chen, Samsung, US; Jingtong Hu, University of Pittsburgh, US; Weidong Shi, University of Houston, US; Lei Ju, Shandong University, CN
- **ABC-FHE: A Resource-Efficient Accelerator Enabling Bootstrappable Parameters for Client-Side Fully Homomorphic Encryption**
  Sungwoong Yune, Hyojeong Lee, Adiwena Putra, Hyunjun Cho, Duong Cuong, Jaeho Jeon, Joo-Young Kim, Korea Advanced Institute of Science and Technology, KR
- **SeDA: Secure and Efficient DNN Accelerators with Hardware/Software Synergy**
  Wei Xuan, Zihao Xuan, Yuzhong Jiao, Luhong Liang, The Hong Kong University of Science and Technology, CN; Zhongrui Wang, Southern University of Science and Technology, CN; Lang Feng, Sun Yat-sen University, CN; Ning Lin, The University of Hong Kong, CN; Rongliang Fu, Tsung-Yi Ho, The Chinese University of Hong Kong, HK

- **Guarder: A Stable and Lightweight Reconfigurable RRAM-Based PIM Accelerator for DNN IP Protection**
  Ning Lin, The Yi Li, Jiankun Li, Jichang Yang, Yangu He, Xiaojuan Qi, The University of Hong Kong, HK; Yukui Luo, Binghamton University, US; Dashan Shang, Xiaoming Chen, Institute of Computing Technology, Chinese Academy of Sciences, CN; Zhongrui Wang, Southern University of Science and Technology, CN
- **Quorum: Zero-Training Unsupervised Anomaly Detection Using Quantum Autoencoders**
  Jason Ludmir, Sophia Rebello, Tirthak Patel, Rice University, US; Jacob Ruiz, Stanford University, US

Session Chair(s): Jack Miskelly , Queen's University; Stefano Di Carlo, Politecnico di Torino

WELCOME TO THE SILICON RODEO: WRANGLING TRANSISTORS, TAMING YIELD, AND RIDING THE 3D PACKAGING FRONTIER

Time: 10:30 AM - 12:00 PM

Topic Area: EDA

Session Type: Research Manuscript

Room: 3003,Level 3

Description: Ready for a wild ride through the next frontier of semiconductor design? From wrangling transistor layouts in CFET and Flip-FET to taming the unruly beasts of yield prediction with AI-driven multi-agent analysis, we're corralling the toughest challenges in modern VLSI. We'll dive into 3D chiplet packaging with YAP's ultra-fast yield modeling, lasso post-exposure bake accuracy with SDM-PEB, and now, with ChipletEM, we're putting the spurs to electromigration signoff in 2.5D and 3D integration. Saddle up as we rustle up the best innovations in chip design, ensuring your circuits don't get bucked off the road to tape-out!

- **Mitigating Routability Problems in Complementary-FET-Based VLSI Designs**
  Junghyun Yoon, Heechun Park, Ulsan National Institute of Science and Technology (UNIST), KR
- **Design and Technology Co-Optimization Utilizing Flip-FET (FFET) Standard Cells**
  Jaehoon Ahn, Taewhan Kim, Seoul National University, KR
- **Multi-Agent Yield Analysis for Circuit Design**
  Haiyan Qin, Jing Kou, Liang Zhang, Wang Kang, Beihang University, CN; Wei Xing, The University of Sheffield, GB
- **YAP: Yield Modeling and Simulation for Advanced Packaging**
  Zhichao Chen, Puneet Gupta, University of California, Los Angeles, US
- **SDM-PEB: Spatial-Depthwise Mamba for Enhanced Post-Exposure Bake Simulation**
  Ziyang Yu, Peng Xu, Zixiao Wang, Bei Yu, Martin Wong, The Chinese University of Hong Kong, HK; Binwu Zhu, Southeast University, CN; Qipan Wang, Yibo Lin, Runsheng Wang, Peking University, CN
- **ChipletEM: Physics-Based 2.5D and 3D Chiplet Integration Electromigration Signoff Tool Using Coupled Stress and Thermal Simulation**
  Zeyu Sun, Weijie Tong, Xiaoning Ma, He Cao, Jianyun Liu, Zhiqiang Li, Qinzhi Xu, Institute of Microelectronics Chinese Academy of Sciences, CN

Session Chair(s): Qi Sun, Zhejiang University; Ing-Chao Lin, National Cheng Kung University

CHIPS AND SYSTEMS FOR AI: GAINS, DRAINS AND THE UNCHARTED ROAD AHEAD

Time: 10:30 AM - 12:00 PM

Topic Area: AI

Session Type: Research Panel

Room: 3012, Level 3

Description: The rapid evolution of artificial intelligence (AI) marks a transformative leap in technology, reshaping industries and influencing everyday life. AI has emerged as a cornerstone of innovation, enhancing productivity and unlocking new possibilities across diverse domains. The integration of advanced deep learning (DL) models, vast datasets, and powerful hardware is revolutionizing the computing industry. Over the past decade, advancements such as convolutional neural networks and transformers have broadened AI's applications, from vision and language to sophisticated generative tasks. Today, large language models (LLMs), equipped with trillions of parameters and trained on terabytes of data, exemplify this progress.

Accompanying these developments are significant hardware breakthroughs. For instance, modern GPUs achieve an astonishing performance of 40 Peta Ops, representing exponential improvements over the last decade. Energy efficiency has also seen significant progress, with cutting-edge research prototypes delivering over 100 TOPS/W.

We stand at a pivotal moment, where reflection on past achievements enables us to celebrate milestones and identify key contributors. At the same time, this understanding helps shape a roadmap for the future, highlighting challenges and exploring innovative solutions. Critical questions driving these discussions include:

1. Dual-edged nature of AI
   - While LLMs and AI advancements have transformed our lives, have they genuinely boosted productivity, or have they primarily fueled the spread of misinformation?
   - Have we sacrificed security and overlooked ethical biases in the rush for rapid progress? What critical lessons can we learn from these past missteps?

2. Have we reached the limits of AI scaling?
   - Can models and hardware continue to grow at their current pace, or is the era of exponential scaling nearing its end?
   - Are smaller models the answer to high computational demands?
3. Is hardware innovation keeping up?
   - Can hardware performance sustain the rapid advancements in DL models?
   - What emerging hardware technologies could disrupt the future? Are technologies like In-memory computing, Neuromorphic computing promising or just a hype?
4. Specialization vs. Generalization
   - Will the future belong to specialized models tailored to specific domains, or will general-purpose models dominate? How transformative are technologies such as Mixture of Experts (MoE)?
   - Should future DL hardware prioritize bespoke solutions, or is flexibility key to serving diverse applications?
5. Economic Viability
   - Can AI applications justify their soaring costs in both the short and long term?
   - Are companies overinvesting in AI without clear paths to economic sustainability?

This panel discussion will convene experts from industry and academia with extensive experience in deep learning systems and product development. By reflecting on AI's priorities and lessons from the past decade, the panel will explore strategies to address pressing challenges in AI development. These insights aim to pave a roadmap for AI's future, fostering a balanced and innovative approach to technological advancement.

Organizer(s): Rangharajan Venkatesan, Ben Keller, Nvidia, US

Moderator: Yingyan Lin, Georgia Institute of Technology, US

Speakers: Anand Raghunathan, Purdue University, US; Bora Nikolic, University of California, Berkeley, US; Brucek Khailany, Nvidia, US; Edith Beigne, Meta, US; Jaydeep Kulkarni, University of Texas Austin, US; Suk Hwan Lim, Stealth Start-Up

QUANTUM THREATS, DISAGGREGATED ARCHITECTURES, AND CRYPTOGRAPHY LEAKAGES

Time: 10:30 AM - 12:00 PM

Topic Area: Design

Session Type: Special Session (Research)

Room: 3010, Level 3

Description: In this session, we will present the security threats, and associated challenges in defending against such threats in the context of the emerging computing platforms of future such as quantum computing, disaggregated architectures. We will present systems and network level threats for disaggregated architecture. We will also explore how cryptography is being used across hardware, software, data planes, what are the related research challenges against multi-cryptography leakages, against cryptographically relevant quantum computing (CRQC), and remediation approaches.

- **Towards Secure Data Management Using Multi-Cryptographic Solutions**
  Sharad Mehrotra, UC Irvine, US
- **Security Opportunities and Challenges for Disaggregated Architectures**
  Elisa Bertino, Purdue University, US
- **Quantum-Resistant Security: PQC Readiness and Research Challenges**
  Ashish Kundu, Cisco, US

Organizer(s): Barry Mishra, University of California, Irvine, US

AUTOMATED PLATFORM FOR CREATING OPTIMIZED 2.5D AND 3D CHIPLET DIE-TO-DIE INTERCONNECT IP SOLUTIONS FOR EXTREMELY HIGH BANDWIDTH APPLICATIONS

Time: 11:15 AM - 11:45 AM

Session Type: Exhibitor Forum

Topic Area(s): Design

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The requirement for extremely high bandwidth chiplet interconnectivity in 2.5D and 3D packaging technologies has surged, driven by exponential growth in computing performance required for Artificial Intelligence and Machine Learning (AI/ML) applications. These new chiplet architectures have created an urgent need for high-performance, customizable die-to-die (D2D) interconnect IP solutions. This presentation explores the application of an automated analog design platform, specifically the Blue Cheetah Adaptive Interconnect Platform (AIP), to accelerate the development and optimization of D2D interconnect IP for extremely high bandwidth chiplet ecosystems. We will discuss how AIP's parameterizable generator scripts can automate the creation of layout, schematic, and simulation environments for D2D interconnect circuits. The framework's ability to encode design methodologies and leverage computer resources for iterative design and verification processes will be highlighted. We'll demonstrate how this approach can significantly reduce turnaround time from circuit design to tape-out in advanced FinFET nodes. The presentation will cover key challenges in high-bandwidth D2D interconnect design, including bandwidth density, energy efficiency, and signal integrity. Case studies will illustrate the application of AIP to create UCIe compatible D2D PHYs, showcasing quick customization for various data rates, I/O configurations, and packaging types. By demonstrating the power of automated analog design tools in creating flexible, high-performance D2D interconnect IP, this presentation aims to highlight a path forward for accelerating chiplet ecosystem development and enabling more efficient heterogeneous integration solutions for extremely high bandwidth applications.

Speakers: Elad Alon, Blue Cheetah Analog, US

BEYOND AUTOMATION: HOW AGENTIC AI IS REINVENTING CHIP DESIGN AND VERIFICATION

Time: 11:15 AM - 12:00 PM

Session Type: TechTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Semiconductor innovation is at a critical juncture, demanding next-generational methods to overcome rising complexities, shorter design cycles, and intense competitive pressures. Traditional EDA tools are constrained by manual processes and limited intelligence, but what if we could transcend these limitations?

Enter AI Agents—the AI solution leveraging large language models and advanced algorithms to continue to improve themselves. In this talk, Prof. William Wang, Founder & CEO of ChipAgents, will introduce how AI agents go beyond traditional EDA automation, embedding agentic intelligence capable of independently handling hardware modeling, constraint-solving, automated debugging, testbench generation, and even proactive design optimization. Highlights include Use Cases, Scalability & Reliability: Case studies illustrating substantial productivity improvements, enhanced design quality, and accelerated time-to-market achieved by leading semiconductor enterprises deploying AI Agents. AI Agents in Action: Real-world scenarios demonstrating how AI agents autonomously identify critical bugs, optimize RTL designs, and significantly shorten verification cycles.

Speaker: William Wang, ChipAgents, US

SIEMENS

Time: 12:00 PM - 12:30 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: TBA

Speakers: TBA, US

WEDNESDAY ENGINEERING TRACKS POSTER RECEPTION

Time: 12:15 PM - 1:15 PM

Session Type: Engineering Poster

Room: Engineering Posters, Level 2 Exhibit Hall

A DFT PARALLEL TEST TECHNOLOGY

Qi Cheng, Zhijun Long, Minqiang Peng, Tianjiao Wang, Pengfei Xi, Chenyang Zhang, Keqing Ouyang, Guohua Zhou, Xianjun Zeng, Sanechips Technology Co., Ltd, CN

A NEW VIRTUAL IP MODELING METHODOLOGY FOR RE-USABILITY IN HETEROGENEOUS VIRTUAL PLATFORMS

Yoonjoong Oh, DongYoung Lee, Jinyoung Hwang, Haeun Kim, Seungik Ha, Jinbeom Kim, Jongsung Park, Kyungsu Kang, Silwan Jang, Samsung, KR

A SOLUTION FOR INTERMITTENTLY AND FASTLY POWER ON REPAIR

Minqiang Peng, Feilong Pan, Tianjiao Wang, Junhua Qin, Hu Hai, Lei Chen, Keqing Ouyang, Guohua Zhou, Sanechips Technology Co.,Ltd, CN; Jian Yu, Fengfeng Tang, Zhuo Wang, Synopsys, CN

A X-MASK CHIP FAST BINNING TECHNOLOGY

Jiawei Wang, Minqiang Peng, Lei Chen, Keqing Ouyang, Guohua Zhou, Sanechips Technology Co.,Ltd, CN

ACCELERATING ANALOG CONNECTIVITY VERIFICATION WITH JASPER: COMPARING FORMAL METHODS TO MIXED SIMULATION

Davide Sanalitro, Edoardo Bollea, STMicroelectronics, IT

WEDNESDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

ACCELERATING CHIP DESIGN WITH AI-POWERED ADDITIVE LEARNING FOR DEEP SUB-MICRON TECHNOLOGIES
Mohamed Atoua, Ajaj Ansari, Siemens, IN; Amit Bansal, Raju Raasa, Vishal Kulshrestha, Microchip, IN

ACCELERATING IR SIMULATION WORKFLOWS WITH AUTOMATED SETUP AND RESULTS DATA VISUALIZATION TOOLS FOR DIGITAL DESIGNS USING VOLTUS PLATFORM
Ninad Khire, Yash Zavar, Kavithaa Rajagopalan, Keerthi Nori, Murtaza Tankiwala, Rishabh Singh, Subhadeep Ghosh, Texas Instruments, IN

ACTIVITY-BASED POWER DENSITY OPTIMIZATION
Sravanthi Gajjala, Karanvir Singh, Rakesh Kumar, Nilabh Srivastava, Intel, IN; Vinesh Jayaraman, Cadence Ashish Kumar, Satish Sethuraman, Intel, IN

AGENTIC AI APPROACH TO OPTIMIZE FRONT-END EDA TOOLS FLOW
Nitin Pundir, Maya Safieddine, Arvind Haran, Rich Carbone, Frank Wallingford, Ali El-Zein, Viresh Paruthi, Dan Coops, IBM, US

AN ADVANCED MULTI-VECTOR OPTIMIZATION METHODOLOGY TO ENHANCE POWER PERFORMANCE IN SCALED-DOWN TECHNOLOGY NODES.
Lakshmidas K, Gowry Shanmugam, Sravanthi Gajjala, Cadence Design Systems, Inc., IN

AN EFFICIENT METHODOLOGY FOR MULTI-PVT EMIR ANALYSIS OF LARGE SOCS
Ramesh Agarwal, Pratik Shah, Nvidia, IN; Anusha Vemuri, Rajvi Shah, Emmanuel Chao, Santosh Santosh, Nvidia, US; Anush Sharma, Shreya Sashi, Naveen B, Ansys, IN

AUTOMATED GENERATION OF ISO 21434 VERIFICATION WORK PRODUCTS
Mohit Shrivastava, Prachi Mishra, Texas Instruments, IN

AUTONOMOUS PHYSICAL DESIGN: ACCELERATING ASIC DESIGN USING MACHINE LEARNING
Sarah Ahmad, Jason Chow, Ayan Datta, Western Digital, IN

AUTOMATED MODELLING AND ASSERTION GENERATOR FOR VERIFYING ANY GENERIC COMPLEX IO CONTROLLERS
Ayush Jodh, Kumar Singh, Parthasarathy Ramesh, Harish Maruthiyodhan, Texas Instruments, IN

AUTOMATION OF SHMOO ENGINE BASED PRE-SI BDI TESTING
Mohit Shrivastava, Prachi Mishra, Rakesh Bansal, Krishan Prajapat, Texas Instruments, IN

BOOSTING LOW POWER VERIFICATION METHODOLOGY: INTRODUCING POWER-AWARE FORMAL PROPERTY VERIFICATION INTO THE FLOW
Gianluca Rigano, David Vincenzoni, STMicroelectronics, IT; Patrick Blestel, Synopsys, FR

BUILDING A PARALLEL SIMULATION KERNEL FOR FASTER & BETTER VIRTUAL PLATFORMS
Jakob Engblom, ASTC, SE

CDC-RDC INTER-OPERABLE COLLATERAL STANDARDIZATION
Anupam Bakshi, Agnisys Inc., US; Bill Gascoyne, Blue Pearl Software, US; Don Mills, Microchip Technology Inc, US

CLOCK H-TREE EXPLORATION IN BSPDN
Jongbeom Kim, Dayeon Cho, Wook Kim, Ki-ok Kim, Hyung-Ock Kim, Samsung, KR

CONFIDENTIALITY ASSURANCE: A KEY COMPONENT OF HARDWARE SECURITY
Varun Sharma, Vikas Sachdeva, Vinod Viswanath, Real Intent Inc., US

CONTEMPORARY PPAS OPTIMIZATION STRATEGIES IN PHYSICAL IMPLEMENTATION OF DIGITAL SOCS – A CASE STUDY
Sukhmani Virk, Utkarsha Suman, Ben Thomas, Megha Mendu, Murtaza Tankiwala, Kavithaa Rajagopalan, Texas Instruments, IN

DESIGN FOR TIME INTERLEAVING OF DATA USING S UB-SAMPLING CLOCKS
Aradhana Kumari, STMicroelectronics, FR

DESIGN-FOR-VERIFICATION ARCHITECTURE TO SHIFT-LEFT TTM AND ALIGN TEST CODEBASE IN MULTI-CHIPLET SOCS
David Akselrod, Alex Branover, Rob Pelt, Ananth Pallapothu, Advanced Micro Devices (AMD), US; Nicola Nicolici, McMaster University, CA

EARLY CLOCK NETWORK JITTER ESTIMATION
Tusharkant Mishra, Pradeep Kothari, Ayan Datta, Western Digital India Private Limited, IN

EASY AI FOR STA TEAMS
Tim Helvey, Marvell, US

ENHANCEMENTS IN CELL-AWARE UDFM MODELS TO OPTIMIZE THE DEVELOPMENT FLOW OF CUSTOM MACROS/IP AND STANDARD CELL LIBRARIES
Ravi J N, Pramod Gayakwad, NXP Semiconductor, IN

ENHANCING DESIGN QUALITY THROUGH A HIGH-LEVEL SYNTHESIS FLOW IN NEURAL NETWORK-BASED KEYWORD SPOTTING SYSTEMS
Gianluca Rigano, Luca Francesco Perroni, Mario Blangiforti, Savino Bellopede, Paolo Mazzetti, Enrico Papa, Michele Palma, Giuseppa Maria Pino, STMicroelectronics, IT

ESD EDA VERIFICATION FLOW APPLIED TO SMART POWER IC'S
Chiara Bielli, Stefano Angeli, STMicroelectronics, IT

EXPLORING THE LATENT SPACE IN A VARIATIONAL AUTO ENCODER WHEN ADDRESSING LOCAL LAYOUT EFFECTS
Rafael Toche Pizano, Richard Wachnik, Michael Monkowski, IBM, US

WEDNESDAY ENGINEERING TRACKS POSTER RECEPTION (continued)

FROM BLOCK, CHIP TO SYSTEM - A COMPREHENSIVE FLOW FOR LARGE FPGA DYNAMIC POWER INTEGRITY SIGN-OFF

Dengji Dong, Chenxu Guo, Yige Technology Co., Ltd., CN; Yiting Lin, Yahui Li, Ansys, CN

HEATSYNC: MACHINE LEARNING-DRIVEN FLOORPLANNING FOR OPTIMIZED POWER INTEGRITY AND THERMAL INTEGRITY IN ADVANCED PACKAGES

Jisoo Hwang, KiHun Ok, SoYoung Kim, Sungkyunkwan University, KR; Myunghoon Lee, Ki Wook Jung, Ansys, KR; Subodh Deodhar, Ansys, IN

HIERARCHICAL EARLY LATCHUP CHECKING FLOW

Yamini Ravishankar, Sanghmitra Jha, Greg Ford, Marvell, US

HSTAF: HIERARCHICAL STATIC TIMING ANALYSIS FLOW

Pardhu Pavan, Ayan Datta, Himanshu Bansal, Vikash T, Western Digital, IN

I/O POWER GRID ANALYSIS METHODOLOGY

Daniel Kim, Marvell Technology, US

IMPROVING DIGITAL DESIGN PERFORMANCE AND AREA USING DSO.AI

Michele Battista, Mario Blangiforti, Luca Francesco Perroni, Luca Pulvirenti, Massimo Bertoletti, Synopsys, IT

INNOVATIVE AND COST-EFFECTIVE APPROACH TO ESD RELIABILITY VERIFICATION IN THE CLOUD

Gazal Single, Siemens, IN; Ertugrul Demircan, NXP Semiconductors, US

IP-REPORT: METHODOLOGY TO IDENTIFY SIMPLE YET EFFECTIVE MODULE BASED POWER SAVING TECHNIQUES

Suseela Budi, Praveen Narendranath, Qualcomm, IN; Sanjeeth Reddy Ayanala, Qualcomm, US; Anbar Hicham, Siemens, MA; Anmol Garg, Mohammed Fahad, Manish Kumar, Vishal Kashyap, Vishnu Kanwar, Divya Bareja, Siemens, IN

MACHINE LEARNING ACCELERATED DISTRIBUTED COMPUTING PLACE AND ROUTE FRAMEWORK FOR HIGH PERFORMANCE CPU DESIGNS

Loknath Moogi, Gowry Shanmugam, Riya Raj, Mohit Gupta, Cadence Design Systems, Inc., IN; Sivaraman P, Intel Corporation, IN

METHOD OF STATIC TIMING ANALYSIS FOR DUAL EDGE TRIGGERED PULSED LATCHES

Kerim Kalafala, Hemlata Gupta, Manish Verma, IBM, IN

MITIGATING ROUTING CONGESTION IN AUTOMOTIVE SOCS WITH ML BASED POWER GRID OPTIMIZATION

Govind Pal, ST Microelectronics, IN; Amit Jangra, Harshul Bansal, Ansys, IN

NOVEL METHODOLOGY TO ADDRESS ESD VERIFICATION COMPLEXITY OF 2.5D/3D-IC DESIGNS

Hirotaka Yamazaki, Socionext Inc., JP

ON-DIE POWER NOISE IMPACT ON HIGH-SPEED SIGNAL INTEGRITY (SI) OF PHOTONICS COMPUTING CHIP BASE ON 3D HETEROGENEOUS INTEGRATION

Xinyuan Miao, Yongjie Zhu, Grant Zhang, Wayne Wu, PhotonEra, CN; Henry He, Johnny Feng, Tao Wang, Xiaodong Wang, Ansys, CN

PRE-VALIDATION TOOL: MINIMIZING ERRORS, MAXIMIZING EFFICIENCY

Samvedna Jha, Shruthi Ravindra, Utkarsh Chitransh, IBM, IN

REDUCING HIGH DI/DT SIMULTANEOUS SWITCHING NOISE IN ADVANCED MULTIPROCESSOR SOCS

Govind Pal, ST Anil Yadav, ST Microelectronics, IN; Amit Jangra, Harshul Bansal, Ansys, IN

REDUCING TOP LEVEL VERIFICATION CYCLE OF HIGH FREQUENCY PLLS WITH ENHANCED FAST-SPICE TECHNOLOGY

Ankit Gupta, Atul Bhargava, Nitin Jain, Ankur Bal, Anil Dwivedi, STMicroelectronics, IN; Prayes Jain, Cadence Design Systems, Inc., IN

SIGN-OFF CHALLENGES AND SOLUTIONS IN POWER INTEGRITY AND RELIABILITY ANALYSIS OF 2.5DIC SILICON INTERPOSER

Jiajun Zhao, Guifang Chen, Yuming Sun, Pengyue Yin, Shanghai Enflame Intelligence Technologies Co.,Ltd, CN; Xiaodong Wang, Yiting Lin, Ansys, CN

SILICON LIFECYCLE MANAGEMENT IN AUTOMOTIVE DESIGN

Rajnish Garg, Amerjeet Kumar, Harshil Upadhyay, Anil Yadav, STMicroelectronics, IN

SIGMAAV: HIGH GLOBAL AND LOCAL NOISE COVERAGE SOLUTION FOR POWER INTEGRITY SIGNOFF

Anusha Vemuri, Vishal Malik, Emmanuel Chao, Santosh Santosh, Nvidia Corporation, US; Chidambaram Rakkappan, Ansys, CA; Ed Deeters, Ansys, US

SINGLE CORNER MIXED VOLTAGE FUNCTIONAL NOISE ANALYSIS

Steven Kurtz, Michael Sitko, Sanjay Upreti, IBM, US; Rahul Rao, Ajith Chandrasekaran, IBM, IN

STA DASHBOARD: LEVERAGING DATA ANALYTICS FOR EFFECTIVE STATIC TIMING ANALYSIS

Manjunath Nayak, Subhash Uppala, Anoop Singh, Ayan Datta, Western Digital, IN

THERMAL AWARE DESIGN OPTIMIZATIONS AND SIGNOFF USING RHSC-ELECTROTHERMAL

Rajvi Shah, Emmanuel Chao, Santosh Santosh, Nvidia, US; Chris Ortiz, Ansys, US; Ansys, US; Vaibhav Rajput, Ansys, CA

UNLOCKING THE POWER OF AI-BASED VERIFICATION APPS FOR AN INNOVATIVE AND EFFICIENT DIGITAL VERIFICATION FLOW

Davide Sanalitro, STMicroelectronics, IT

AI BOOSTER FOR R&D, EDGE COMPUTING, CHIPLETS, AND SUSTAINABILITY

Time: 1:00 PM - 1:45 PM

Topic Area(s): AI

Session Type: SKYTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Description: Artificial Intelligence (AI) is transforming Research and Development (R&D) by accelerating discovery, optimizing resources, and enhancing decision-making. Edge AI, which processes data closer to its source, reduces latency and energy consumption, promoting sustainability. Chiplet technology, involving smaller integrated circuits combined into larger systems, offers improved performance, scalability, and cost-efficiency. STMicroelectronics is exploring chiplets to advance semiconductor solutions. Amidst climate change, STMicroelectronics is committed to sustainable technologies and responsible products that support decarbonization and digitalization. Integrating AI into R&D, deploying Edge AI, and utilizing chiplets, while addressing sustainability, forms a comprehensive strategy for future advancements, ensuring technological progress and environmental responsibility.

Speaker: Serge Nicoleau, STMicroelectronics, US

A LOOK INTO THE FUTURE OF VERIFICATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): Front-End Design

Session Type: Engineering Track

Room: 2008, Level 2

Description: The verification landscape for integrated circuits continues to evolve rapidly as design complexity grows exponentially. This session brings together industry experts to explore emerging trends and technologies that are reshaping functional verification. Four distinguished speakers will present their insights on key developments including Portable Stimulus Standard (PSS), multi-language verification environments, formal verification methodologies, and cloud-based verification solutions.

Through these presentations, attendees will gain valuable insights into how these complementary approaches are converging to address the verification challenges of next-generation IC designs. Join us for a forward-looking discussion on how the verification landscape will evolve to meet the demands of tomorrow's semiconductor industry.

Organizer(s): Duscia Glisic, Veriest Solutions Ltd., RS

Moderator: Dusica Glisic, Veriest Solutions Ltd., RS

Speakers: Matthew Ballance, Advanced Micro Devices (AMD), US; Thorsten Klose, Infineon Technologies, DE; Avner Landver, Intel Corporation, IS; Jean-Christophe Glas, Arm Ltd., US

KEEPING THE GUARD UP WITH SECURITY ACROSS THE BOARD

Time: 1:30 PM - 3:00 PM

Topic Area(s): Back-End Design

Session Type: Engineering Track

Room: 2010, Level 2

Description: In today's fully connected world, attacks on computing and non-computing connected systems are becoming increasingly common. Often, those attacks severely impact the victims. To address such problems, the research community is aggressively working on various aspects of security. In the first talk of the session, the speaker will discuss utilizing the 3D heterogeneous integration technology to address the semiconductor supply-chain security issues. The second talk will be about the problems and solutions in the context of enhanced assurance for the FPGA-centric EDA tools. The third presenter will discuss the challenges for adopting the Quantum resistant cryptography in the hardware level. In the fourth topic, the speaker will discuss about secure Deep-Learning based EDA flows, because ML-assisted EDA tools are also susceptible to the security issues.

Organizer(s): Sabya Das, Synopsys, US

Moderator: Sabya Das, Synopsys, US

Speakers: Ankur Srivastava, University of Maryland, College Park, US; Lee Lerner, Georgia Institute of Technology, US; Siddharth Garg, New York University, US; Ashish Kundu, Cisco, US

NEUROMORPHIC TESTBEDS: PIONEERING ENERGY-EFFICIENT COMPUTING FOR THE FUTURE

Time: 1:30 PM - 3:00 PM

Topic Area(s): IP

Session Type: Engineering Track

Room: 2012, Level 2

Description: Neuromorphic computing is an emerging paradigm that emulates the computational architecture of the brain with significant performance savings compared to conventional digital architectures. Innovative hardware design will be at the forefront of future computing systems that utilize new and increasingly diverse components. Neuromorphic computing, holds transformative potential for revolutionizing computing across various applications, including artificial intelligence, edge computing, and scientific computing with high energy-efficiency. Large-scale neuromorphic testbeds are essential to engage a larger community and enable rapid prototyping and testing of novel algorithms and systems.

The proposed special session includes five short talks from experts from academia and industry that will highlight latest research efforts to design and implement diverse neuromorphic testbeds, from digital, mixed-signal, analog to beyond-CMOS approaches. The brief presentations will be succeeded by a panel discussion addressing the challenges and opportunities associated with next-generation neuromorphic systems.

Organizer(s): Suma Cardwell, Sandia National Laboratories, US

Moderator: Suma Cardwell, Sandia National Laboratories, US

Speakers: Craig Vineyard, Sandia National Laboratories, US; Rajit Manohar, Yale University, US; Hector Gonzalez, SpiNNcloud, DE; Gert Cauwenberghs, University of California, San Diego, US; Xiaoxuan Yang, University of Virginia, US; Martin Lueker-Boden, Western Digital Corporation, US

FLATTERING SPLATTING: GAUSSIAN SPLATTING, VIDEO PROCESSING, AND DIFFUSION

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: This session is about 3D video processing, diffusion, Gaussian splatting, and their memory optimizations. As research into deep learning grows, often people have found that the models used in deep learning are transitive to applications in vision computing, thus creating a cross-disciplinary experience. We cover hardware-efficient diffusion acceleration, 3D video generation models, and 3D Gaussian splatting. After our 3 papers that focus on Gaussian splatting, we conclude with a paper about diffractive optical neural network, using an emergent technology technique to attack the issues of speed and energy efficiency.

- **MHDiff: Memory-and Hardware-Efficient Diffusion Acceleration via Focal Pixel Aware Quantization**
  Chunyu Qi, Xuhang Wang, Ruiyang Chen, Yuanzheng Yao, Naifeng Jing, Chen Zhang, Xiaoyao Liang, Zhuoran Song, Shanghai Jiao Tong University, CN Jun Wang, Zhihui Fu, OPPO Research Institute, CN
- **Harnessing Conventional Video Processing Insights for Emerging 3D Video Generation Models: A Comprehensive Attention-Aware Way**
  Tianlang Zhao, Jun Liu, Xingyang Li, Li Ding, Jinhao Li, Shuaiheng Li, Jinbo Hu, Guohao Dai, Shanghai Jiao Tong University, CN
- **StreamingGS: Voxel-Based Streaming 3D Gaussian Splatting with Memory Optimization and Architectural Support**
  Chenqi Zhang, Yu Feng, Jieru Zhao, Guangda Liu, Chentao Wu, Minyi Guo, Shanghai Jiao Tong University, CN Wenchao Ding, Fudan University, CN
- **GauRast: Enhancing GPU Triangle Rasterizers to Accelerate 3D Gaussian Splatting**
  Sixu Li, Yingyan (Celine) Lin, Georgia Institute of Technology, US; Ben Keller, Brucek Khailany, Nvidia, US
- **Local-GS: An Order-Independent Gaussian Splatting Training Accelerator Exploiting Splat Locality**
  Yiyang Sun, Qinzhe Zhi, Yiqi Jing, Le Ye, Ru Huang, Tianyu Jia, Peking University, CN
- **Multi-Dimensional Reconfigurable, Physically Composable Hybrid Diffractive Optical Neural Network**
  Ziang Yin, Yu Yao, Jeff Zhang, Jiaqi Gu, Arizona State University, US

Session Chair(s): Yonggan Fu, Georgia Institute of Technology, NVIDIA; Bokyung Kim, Rutgers University

INNOVATIVE TECHNIQUES FOR ANALOG CIRCUIT SIMULATION AND OPTIMIZATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3003, Level 3

Description: Circuit simulation is essential for analog circuit design, but suffers from large computational costs when dealing with large-scale or advanced-technology circuits. This session includes the cutting-edge techniques for the hard-core problems of circuit simulation and optimization. They address the challenges on post-layout SPICE simulation, RF circuit simulation, and the simulation based analog circuit optimization. The innovative ideas are presented to accelerate the simulation process, optimize the core of equation solvers, reduce memory cost, and enable optimization speedup for circuit sizing.

- **PiSPICE: Accelerating Post-Layout SPICE Simulation via Essential Parasitic Identification**
  Zhou Jin, Jing Li, China University of Petroleum-Beijing, CN; Jian Xin, Tianjia Zhou, Zuochang Ye, Tsinghua University, CN; Xiao Wu, Huada Empyrean Software Co. Ltd, CN; Dan Niu, Southeast University, CN
- **Me-MPK: Accelerating Krylov Subspace Solvers via Memory-Efficient Matrix-Power Kernel**
  Haozhong Qiu, Chuanfu Xu, Jianbin Fang, Shengguo Li, Yue Ding, Yue Wang, Zhimeng Han, Yonggang Che, Jie Liu, National University of Defense Technology, CN; Liang Deng, CN Jian Zhang, Zhe Dai, China Aerodynamic Research and Development Center, CN
- **New Time-Domain Preconditioners for HB Jacobian of RF Circuits**
  Chenyi Tan, Yangfeng Su, Xuan Zeng, Fan Yang, Fudan University, CN
- **Efficient Recycling Subspace Truncation Method for Periodic Small-Signal Analysis**
  Yuncheng Xu, Fan Yang, Yangfeng Su, Fudan University, CN
- **MemSens: Significantly Reducing Memory Overhead in Adjoint Sensitivity Analysis Using Novel Error-Bounded Lossy Compression**
  Chenxi Li, Yihang Feng, Fuxing Deng, Weifeng Liu, Zhou Jin, China University of Petroleum-Beijing, CN; Dingwen Tao, Institute of Computing Technology, Chinese Academy of Sciences, CN
- **MARIO: A Superadditive Multi-Algorithm Interworking Optimization Framework for Analog Circuit Sizing**
  Wangzhen Li, Yuan Meng, Ruiyu Lyu, Changhao Yan, Keren Zhu, Zhaori Bi, Xuan Zeng, Fudan University, CN; Dian Zhou, The University of Texas at Dallas, Fudan University, US

Session Chair(s): Sheldon Tan, University of California, Riverside; Ibrahim (Abe) Elfadel, IBM/ Khalifa University

LOOK BOTH WAYS: NEW DIRECTIONS IN HIGH-LEVEL SYNTHESIS AND APPROXIMATE COMPUTING

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: This session presents 6 exciting papers describing recent advances in high-level synthesis (HLS) and approximate computing. On the HLS front, four papers describe new contributions to HLS-generated asynchronous dataflow circuits; the generation of circuits that perform speculative execution efficiently; the use of multiple clock domains to reduce power; and, automated selection of kernels for hardware acceleration. The last two papers are related to approximate computing. The first of these automates design-space exploration in HLS to identify design points with high potential for area/power savings from approximation. The next introduces an efficient approach for binary-to-unary number conversion.

- **PipeLink: A Pipelined Resource Sharing System for Dataflow High-Level Synthesis**
  Rui Li, Intel Corporation, US; Lincoln Berkley, Rajit Manohar, Yale University, US
- **Optimizing Recovery Logic in Speculative HLS**
  Dylan Leothaud, Jean-Michel Gorius, Université de Rennes, FR; Simon Rokicki, Irisa, FR; Steven Derrien, Université de Bretagne Occidentale, FR
- **AutoClock: Automated Clock Management for Power-Efficient HLS Designs on FPGAs**
  Jiawei Liang, Linfeng Du, Xiaofeng Zhou, Jiang Xu, Wei Zhang, Hong Kong University of Science and Technology, HK; Zhe Lin, Sun Yat-sen University, CN
- **Cayman: Custom Accelerator Generation with Control Flow and Data Access Optimization**
  Youwei Xiao, Fan Cui, Zizhang Luo, Weijie Peng, Yun (Eric) Liang, Peking University, CN
- **ADVISOR: Approximate Computing-Friendly High-Level Synthesis Design Space Explorer**
  Baharealsadat Parchamdar, Benjamin Carrion Schaefer, The University of Texas at Dallas, US
- **Comparison-Free Bit-Stream Generation for Cost-Efficient Unary Computing**
  Faeze Banitaba; Amir Hossein Jalilvand, Sercan Aygun, University of Louisiana at Lafayette, US; M. Hassan Najafi, Case Western Reserve University, US

Session Chair(s): Christian Pilato, Politecnico di Milano

NAVIGATING 3D, CLOCK TREES, AND SHARED LEARNING

Time: 1:30 PM - 3:00 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3006, Level 3

Description: This session highlights advances in 3D IC design and clock tree synthesis (CTS) for improved power and performance. In 3D ICs, 3D-Flow minimizes legalization cell displacement using network flow; DCO-3D uses machine learning to predict and reduce routing congestion; while GNN-MLS mitigates congestion by routing across tiers with metal layer sharing, improving timing while addressing testability issues. For CTS, we explore approaches using front and back-side metal layers and reinforcement learning based "hub" node placement to minimize clock skew, buffering, and wire length. Finally, we look into a privacy-protecting, highly accurate federated learning framework to help advance the use of machine learning in EDA.

- **3D-Flow: Flow-Based Standard Cell Legalization for 3D ICs**
  Yuxuan Zhao, Peiyu Liao, Bei Yu, The Chinese University of Hong Kong, HK
- **DCO-3D: Differentiable Congestion Optimization in 3D ICs**
  Hao-Hsiang Hsiao, Yuan-Hsiang Lu, Sung Kyu Lim, Georgia Institute of Technology, US; Yi-Chen Lu, Anthony Agnesina, Rongjian Liang, Haoxing Ren, Nvidia, US; Pruek Vanna-iampikul, Burapha University, TH
- **GNN-MLS: Signal Routing in Mixed-Node 3D ICs Through GNN-Assisted Metal Layer Sharing**
  Jiawei Hu, Sung Kyu Lim, Georgia Institute of Technology, US; Pruek Vanna-iampikul, Burapha University, TH; Zhen Zhuang, Tsung-Yi Ho, The Chinese University of Hong Kong, HK
- **A Systematic Approach for Multi-Objective Double-Side Clock Tree Synthesis**
  Xun Jiang, Haoran Lu, Jiarui Wang, Zizheng Guo, Heng Wu, Runsheng Wang, Ru Huang, Yibo Lin, Peking University, CN; Yuxuan Zhao, Bei Yu, The Chinese University of Hong Kong, HK; Sung Kyu Lim, Georgia Institute of Technology, US
- **To Tackle Cost-Skew Tradeoff: An Adaptive Learning Approach for Hub Node Selection**
  Lin Chen, Guowei Sun, Qiming Huang, Hu Ding, University of Science and Technology of China, CN
- **FedEDA: Federated Learning Framework for Privacy-Preserving Machine Learning in EDA**
  JoonSeok Kim, Donggyu Kim, Seonghyeon Park, Seokhyeong Kang, Pohang University of Science and Technology (POSTECH), KR

Session Chair(s): Igor Markov, Synopsys; David Chinnery, Siemens Digital Industries Software

NEED A BREAK FROM AI? MEMORY-CENTRIC COMPUTING FOR BEYOND MACHINE LEARNING APPLICATION

Time: 1:30 PM - 3:00 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: Near-memory and in-memory acceleration are emerging as powerful paradigms for addressing computational bottlenecks in data-intensive tasks and have applications beyond ML. This session, a fresh look at the roots, covers acceleration of beyond ML applications using unconventional computing architectures with a focus on in-memroy, near-memory and storage accelerators. More specifically, it includes papers ranging from acceleration of vector similarity search, fully homomorphic encryption, algorithms for mapping and scheduling optimization, and in-cache accelerators with ISA extension.

- **Ares: High Performance Near-Storage Accelerator for FHE-Based Private Set Intersection**
  Haoxuan Wang, Yinghao Yang, Jinkai Zhang, Hang Lu, Xiaowei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN
- **GraphAccel: An In-Storage Accelerator for Efficient Graph-Based Vector Similarity Search Using Page Packing and Speculative Search Optimization**
  Yoonyoung Kwon, Yunjong Boo, Hyungmin Cho, Sungkyunkwan University, KR
- **CIM-BLAS: Computing-in-Memory Accelerator for BLAS**
  Rui Liu, Xiangtan University, CN; Zerun Li, Xiaoyu Zhang, Xiaoming Chen, Yinhe Han, Institute of Computing Technology, Chinese Academy of Sciences, CN; Minghua Tang, Xiangtan University, CN
- **Segmented Angular Pre-Processing for Accurate and Efficient In-Memory Vector Similarity Search**
  Chi-Tse Huang, Jen-Chieh Wang, An-Yeu (Andy) Wu, National Taiwan University, TW; Hsiang-Yun Cheng, Academia Sinica, TW
- **Efficient Weight Mapping and Resource Scheduling on Crossbar-Based Multi-Core CIM Systems**
  Hanjie Liu, Sifan Sun, Haiyan Qin, Wang Kang, Beihang University, CN; Aifei Zhang, Yutong Wu, Minhao Gu, Shihang Fu, Shuaikai Liu, Baosen Liu, Zhicun Research Lab, CN
- **ARCANE: Adaptive RISC-V Cache Architecture for Near-Memory Extensions**
  Vincenzo Petrolo, Flavia Guella, Michele Caon, Guido Masera, Maurizio Martina, Politecnico di Torino, IT; Pasquale Schiavone, École Polytechnique Fédérale de Lausanne, CH

Session Chair(s): Shaahin Angizi, New Jersey Institute of Technology; Dinesh Somasekhar, Intel Corporation

OF CIRCUITS AND SECRETS: EMERGING HARDWARE SECURITY PRIMITIVES AND CRYPTOGRAPHIC ACCELERATORS

Time: 1:30 PM - 3:00 PM

Topic Area(s): Security

Session Type: Research Manuscript

Room: 3008, Level 3

Description: With the increasing complexity of modern hardware systems, ensuring robust security mechanisms is more critical than ever. This session on hardware security introduces emerging security primitives and cryptographic accelerators. The featured papers explore advancements in reliable physical fingerprint-based PUF designs and fluctuation sensing, hybrid verification techniques for hardware security, optimized authentication mechanisms for deep neural network (DNN) accelerators, and novel architectures for computing-in-memory (CIM)-based cryptographic accelerators.

- **AccIMT: A Highly Resource-Efficient and Flexible Poseidon Hash-Based Merkle Tree Architecture**
  Changxu Liu, Hao Zhou, Lan Yang, Yifei Feng, Zheng Wu, Zhuoyuan Yang, Fan Yang, Fudan University, CN; Yinlong Li, Shiyong Wu, Shanghai Academy of Future Internet Technology, CN
- **LeakyDSP: Exploiting Digital Signal Processing Blocks to Sense Voltage Fluctuations in FPGAs**
  Xin Zhang, Jiajun Zou, Yi Yang, Qingni Shen, Zhi Zhang, Zhonghai Wu, Peking University, CN; Yansong Gao, The University of Western Austrilia, CN; Trevor E. Carlson, National University of Singapore, SG
- **FastPath: A Hybrid Approach for Efficient Hardware Security Verification**
  Lucas Deutschmann, Dominik Stoffel, RPTU Kaiserslautern-Landau, DE; Wolfgang Kunz, RPTU Kaiserslautern-Landau, DE; Andres Meza, Ryan Kastner, University of California, San Diego, US
- **Re4PUF: A Reliable, Reconfigurable ReRAM-Based PUF Resilient to DNN and Side Channel Attacks**
  Ning Lin, Yi Li, Yangu He, Songqi Wang, Hegan Chen, Kwunhang Wong, Chuxin Li, Jichang Yang, Yifei Yu, Meng Xu, The University of Hong Kong, HK; Yongkang Han, Zhangjiang lab, Shanghai, CN; Rui Chen, Xiaoming Chen, Xiaoxin Xu, Jianguo Yang, Dashan Shang, Institute of Microelectronics, Chinese Academy of Sciences, CN; Zhongrui Wang, Southern University of Science and Technology, CN
- **ACIM-QMM: Efficient Analog Computing-in-Memory Accelerator for QC-MDPC McEliece Cryptosystem**
  Pingdan Xiao, Zhengmiao Wei, Sichun Du, Wanli Chang, Hong Qinghui, Hunan University, CN
- **AutoSkewBMT: Autonomously Synthesizing Optimized Integrity Authentication Mechanism for DNN Accelerators**
  Rakin Muhammad Shadab, Sanjay Gandham, Mingjie Lin, University of Central Florida, US

Session Chair(s): Gang Qu, University of Maryland; Qian Wang, Intel Corporation

WE HAS TO HAVE THESE HARDWARE ACCELERATOR SYSTEMS FOR DEEP LEARNING!

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3001, Level 3

Description: This session is about hardware accelerator system designs and optimizations for DNNs. As deep learning models become larger and larger, the quest to find the most energy efficient, and throughput optimized hardware platforms to perform model tasks is very important. Here in this session, many hardware platforms are covered. Hydra is a mixture-of-expert inference system using chiplets, SynGPU does its optimizations on GPU. We have 3 other papers that explore many-core architectures. Finally, paper SAGA focuses its optimizations on memory.

- **Hydra: Harnessing Expert Popularity for Efficient Mixture-of-Expert Inference on Chiplet System**
  Siqi He, Haozhe Zhu, Jiapei Zheng, Lizhou Wu, Bo Jiao, Qi Liu, Xiaoyang Zeng, Chixiao Chen, Fudan University, CN
- **SynGPU: Synergizing CUDA and Bit-Serial Tensor Cores for Vision Transformer Acceleration on GPU**
  Yuanzheng Yao, Chen Zhang, Chunyu Qi,; Ruiyang Chen, Naifeng Jing, Xiaoyao Liang, Zhuoran Song, Shanghai Jiao Tong University, CN; Jun Wang, Zhihui Fu, OPPO Research Institute, CN
- **Discovering and Exploiting Untapped Buffer Resources in Many-Core DNN Accelerators**
  Yuchen Wei, Jingwei Cai, Mingyu Gao, Guiming Shi, Kaisheng Ma, Tsinghua University, CN; Sen Peng, Zuotong Wu, Xi'an Jiaotong University, CN
- **PacQ: A SIMT Microarchitecture for Efficient Dataflow in Hyper-Asymmetric GEMMs**
  Ruokai Yin, Yuhang Li, Priyadarshini Panda, Yale University, US
- **MetaDSE: A Few-Shot Meta-Learning Framework for Cross-Workload CPU Design Space Exploration**
  Runzhen Xue, State Mingyu Yan, Ziheng Xiao, Xiaochun Ye, Dongrui Fan, Institute of Computing Technology, Chinese Academy of Sciences, CN; Hao Wu, University of Electronic Science and Technology of China, CN
- **SAGA: A Memory-Efficient \underline{A}ccelerator for \ underline{GA}NN Construction via Harnessing Vertex \ underline{S}imilarity**
  Ruiyang Chen, Xueyuan Liu, Chunyu Qi, Yuanzheng Yao, Yanan Sun, Xiaoyao Liang, Zhuoran Song, Shanghai Jiao Tong University, CN

Session Chair(s): Andreas Herkersdoft, Technical University of Munich; Johannes Maximilian Kuehn, NVIDIA Corporation

GENERATIVE AI IN ELECTRONIC DESIGN AUTOMATION (EDA): REVOLUTION OR RISK?

Time: 1:30 PM - 3:00 PM

Topic Area(s): AI, EDA

Session Type: Research Panel

Room: 3012, Level 3

Description: Generative Artificial Intelligence (AI) is poised to transform Electronic Design Automation (EDA), offering groundbreaking opportunities to enhance how semiconductors are designed and optimized. By automating complex tasks such as circuit layout, synthesis, and verification, AI has the potential to drastically reduce design cycles, improve quality, and unlock innovative solutions that transcend traditional methodologies.

Despite its promise, integrating generative AI into EDA raises significant technical challenges. Concerns about the reliability, robustness, and interpretability of AI-generated designs remain central, particularly for safety-critical applications where the cost of errors is high. There is also the question of whether AI tools can consistently produce results that meet or exceed the quality standards of human-designed circuits. The computational cost and energy requirements for training and deploying AI models raise concerns about scalability and sustainability, especially as designs grow in complexity.

Additionally, AI-driven workflows introduce concerns about security vulnerabilities and intellectual property (IP) privacy. The use of large datasets for model training and the integration of AI in design processes could expose sensitive information or inadvertently introduce exploitable weaknesses into the final designs. Addressing these risks will be essential to ensure trust in AI-driven EDA tools. Furthermore, the adoption of these technologies is set to reshape job skills in the industry, demanding new expertise in AI, data science, and software engineering alongside traditional EDA competencies.

This panel brings together perspectives from leading industry practitioners, academic researchers, and technology innovators to delve into the technical implications of integrating generative AI into EDA workflows. Discussions will focus on the opportunities AI presents for improving efficiency and design quality, the challenges of deploying reliable and interpretable models, addressing security and IP risks, and the evolving skillsets required to work alongside AI-driven tools. Attendees will gain a nuanced understanding of the technical opportunities and hurdles at the intersection of AI and EDA, as well as insights into how the industry is preparing for this transformative shift.

Organizer(s): Rozhin Yasaei, Soheil Salehi, University of Arizona, US

Moderator: Ronald DeMara, University of Central Florida, US

Speakers: Farimah Farahmandi, University of Florida, US; Ivan Kissiov, SiemensEDA, US; Hamid Shojae, ChipStack, US; Matheus Moreira, Meta, US; Benjamin Tan, University of Calgary, CA

BUILDING THE WORKFORCE OF TOMORROW: THE ROLE OF EDA TOOLS IN SKILL UNIVERSITIES

Time: 1:45 PM - 2:15 PM

Topic Area(s): EDA

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: The global semiconductor sector is witnessing a surge in demand for proficient individuals with expertise in VLSI design and fabrication. Skill universities significantly contribute to bridging the divide between academia and industry by integrating advanced EDA tools into their curricula. This forum will showcase best practices, success narratives, and collaborative opportunities for EDA vendors and technical universities. Participants will discover how these tools can foster innovation, enhance student employability, and facilitate academic research that aligns with industry trends.

Speakers: Chandra Sekhar, Centurion University of Technology and Management, US

POSTER GLADIATOR FINALE

Time: 2:00 PM - 3:00 PM

Session Type: Engineering Posters

Room: DAC Pavilion, Level 2 Exhibit Hall

DEEPPCB: TRANSFORMING PCB PLACE & ROUTE THROUGH REINFORCEMENT LEARNING

Time: 2:30 PM - 3:00 PM

Topic Area(s): AI

Session Type: Exhibitor Forum

Room: Exhibitor Forum, Level 1 Exhibit Hall

Description: Today's PCB designers face significant challenges, including component shortages, rapidly evolving design constraints, and intense pressure to deliver results quickly. Traditional manual place-and-route processes frequently involve repetitive, time-consuming tasks that delay development.

In this talk, we introduce DeepPCB, an AI-based tool that learns PCB placement and routing through iterative trial and error, quickly generating DRC-compliant designs. We illustrate DeepPCB's capabilities through a practical use-case involving a complex multi-layer PCB design, demonstrating how this integrated approach significantly reduces design iteration cycles. This helps designers swiftly respond to demanding timelines and component shortages.

Participants will discover how AI-driven tools like DeepPCB enable engineers to spend less time on repetitive tasks and more on strategic, creative aspects of PCB development. The session emphasizes the collaborative potential between human designers and AI, highlighting tangible productivity gains and enhanced adaptability to industry challenges.

Speakers: Alain-Sam Cohen, InstaDeep

ENGINEERING PRESENTATION AWARDS

Time: 3:00 PM - 3:45 PM

Session Type: Engineering Posters

Room: DAC Pavilion, Level 2 Exhibit Hall

BREAKING BARRIERS: COMPUTE-IN-MEMORY FOR TRANSFORMER ACCELERATION

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3001, Level 3

Description: This session highlights groundbreaking innovations in Compute-in-Memory (CIM) architectures designed to accelerate large-scale transformer models and alleviate data transfer bottlenecks. It covers various optimization strategies, from CIM-based solutions for attention computation in large language models (LLMs) to efficient memory management for long-context inference. The session delves into software-hardware co-design techniques, including irregular attention sparsity, outlier-aware quantization, Mixture-of-Experts (MoE) approaches, 3D hybrid bonding, and novel asynchronous execution methods.

- **DIAS: Distance-Based Attention Sparsity for Ultra-Long-Sequence Transformer with Tree-like Processing-in-Memory Architecture**
  Zekai Chen, Yiming Chen, Teng Wan, Tianyi Yu, Yu Wang, Huazhong Yang, Xueqing Li, Tsinghua University, CN
- **AttenPIM: Accelerating LLM Attention with Dual-Mode GEMV in Processing-in-Memory**
  Liyan Chen, Dongxu Lyu,; Zhenyu Li, Jianfei Jiang, Qin Wang, Zhigang Mao, Naifeng Jing, Shanghai Jiao Tong University, CN
- **SplitSync: Bank Group-Level Split-Synchronization for High-Performance DRAM PIM**
  Yoon Byungkuk, Sanghyeok Han, Gyeonghwan Park, Jae-Joon Kim, Seoul National University, KR
- **PIMoE: Towards Efficient MoE Transformer Deployment on NPU-PIM System Through Throttle-Aware Task Offloading**
  Lizhou Wu, Haozhe Zhu, Siqi He, Xuanda Lin, Xiaoyang Zeng, Chixiao Chen, Fudan University, CN
- **Supporting Register-Based Addressing Modes for In-DRAM PIM ISAs**
  Seok Young Kim, Byung Ho Choi, Seon Kim, Korea University, KR; Seokwon Kang, Yongjun Park, Yonsei University, KR
- **OutlierCIM: Outlier-Aware Digital CIM-Based LLM Accelerator with Hybrid-Strategy Quantization and Unified FP-INT Computation**
  Zihan Zou, Shikuang Chen, Chen Zhang, Xing Wang, Zhichao Liu, Haoran Du, Xin Si, Hao Cai,; Bo Liu, Southeast University, CN
- **Near-Memory LLM Inference Processor Based on 3D DRAM-to-Logic Hybrid Bonding**
  Sanghyeok Han, Yoon Byungkuk, Gyeonghwan Park, Jae-Joon Kim, Seoul National University, KR; Choungki Song, Dongkyun Kim, SK hynix, KR
- **SelM: In-Memory Acceleration for Approximate Nearest Neighbor Search**
  Chaoqiang Liu, Yu Huang, Haifeng Liu, Yi Zhang, Xiaofei Liao, Hai Jin, Huazhong University of Science and Technology, CN Dan Chen, Huize Li, National University of Singapore, SG; Wenjing Xiao, Guangxi University, CN

Session Chair(s): Steve Dai, Nvidia; Haitong Li, Purdue University

EXPLORING THE FORMAL FRONTIER FOR VERIFICATION AND VALIDATION

Time: 3:30 PM - 5:30 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3004, Level 3

Description: This session presents the forefront of research in formal verification, driving forward the development of more efficient and reliable tools for modern system validation. It covers cutting-edge approaches, including efficient SAT solvers, symbolic model checking, and logic optimization, aimed at improving the accuracy, scalability, and automation of verification processes. Papers presented delve into innovations like hybrid algorithms for subcircuit identification, SMT counting, and proof obligation refinement, highlighting new frontiers in tackling complex verification challenges.

- **Efficient Rectification Signal Validation for Optimal Functional ECO Patch Generation**
  Tzu-Yu Tung, Chung-Yang (Ric) Huang, National Taiwan University, TW; Yu-Ling Hsu, Shao-Lun Huang, Cadence Design Systems, Inc., TW

- **X-SAT: An Efficient Circuit-Based SAT Solver**
  Yuhang Qian, Zhihan Chen, Xindi Zhang, Shaowei Cai, Institute of Software, China Academy of Science, CN
- **Approximate SMT Counting Beyond Discrete Domains**
  Arijit Shaw, Chennai Mathematical Institute, IN; Kuldeep S Meel, University of Toronto, CA
- **Leveraging Critical Proof Obligations for Efficient IC3 Verification**
  Lingfeng Zhu, Xindi Zhang, Yongjian Li, Shaowei Cai, Institute of Software, Chinese Academy of Sciences, CN
- **Property-Driven Parallel Symbolic Model Checking of LTL**
  Yuheng Su, Yingcheng Li, Qiusong Yang, Yiwei Ci, Institute of Software, Chinese Academy of Sciences, CN; Ziyu Huang, Beijing Forestry University, CN
- **RE3: Finding Refinement Relations with Relational Mapping Abstraction**
  You Li, Guannan Zhao, Yunqi He, Hai Zhou, Northwestern University, US
- **Logic Optimization Meets SAT: A Novel Framework for Circuit-SAT Solving**
  Zhengyuan Shi, The Tiebing Tang, Jiaying Zhu, Sadaf Khan, Qiang Xu, The Chinese University of Hong Kong, HK; Hui-Ling Zhen, Mingxuan Yuan, Huawei, HK; Zhufei Chu, Ningbo University, CN
- **H3Match: A Hybrid Heterogeneous Hypergraph Matching Method for Subcircuit Identification**
  Bohao Li, Qingsong Peng, Zhejiang University, CN; Changhong Wang, Shandong Yunhai Guochuang Cloud Computing Equipment Industry Innovation Co., Ltd., CN; Tianming Ni, Anhui Polytechnic University, CN; Tinghuan Chen, The Chinese University of Hong Kong, Shenzhen, CN; Qi Sun, Cheng Zhuo, Zhejiang University, CN

Session Chair(s): Namrata Shekhar, Synopsys; Enrico Fraccaroli, University of Verona, IT

TITLE: FASTER, SAFER, GREENER: AI-DRIVEN EVOLUTION IN SMART EDGE

Time: 3:30 PM - 5:30 PM
Topic Area(s): Systems
Session Type: Research Manuscript
Room: 3006, Level 3

Description: This session explores AI-driven innovations shaping edge intelligence in acceleration, reliability, and sustainability. It begins with acceleration in 3D point cloud detection, edge-compute-free image compression, and multi-model decentralized federated learning. Reliability is then reinforced with Linux runtime integrity measurement, automated hardware verification, and high-level synthesis with post-implementation. It concludes with sustainability through energy-efficient forecasting and architecture-level power modeling. These innovations drive the next generation of smart edge computing.

- **DAWN: Accelerating Point Cloud Object Detection via Object-Aware Partitioning and 3D Similarity-Based Filtering**
  Dongdong Tang, City Yu Mao, City University of Hong Kong, HK; Weilan Wang, Nan Guan, City University of Hong Kong, HK; Tei-Wei Kuo, National Taiwan University, TW; Chun Jason Xue, Mohamed bin Zayed University of Artificial Intelligence, AE
- **Easz: An Agile Transformer-Based Image Compression Framework for Resource-Constrained IoTs**
  Yu Mao, Jun Wang, Guan Nan, City University of Hong Kong, HK; Jingzong Li, Hang Seng University, HK; Hong Xu, Chinese University of Hong Kong, HK; Tei-Wei Kuo, National Taiwan University, TW; Chun Xue, Mohamed bin Zayed University of Artificial Intelligence, AE
- **MMDFL: Multi-Model-Based Decentralized Federated Learning for Resource-Constrained AIoT Systems**
  DengKe Yan, Yanxin Yang, Mingsong Chen, East China Normal University, CN; Ming Hu, Nanyang Technological University, SG; Xin Fu, University of Houston, US
- **LightRIM: Light Runtime Integrity Measurement for Linux Kernels in Embedded Applications**
  Yili Guo, Zhuoran Ma, Xiangyue Li, Jiajia Huang, Wanli Chang, Hunan University, CN
- **UVLLM: An Automated Universal RTL Verification Framework Using LLMs**
  Yuchen Hu, Junhao Ye, Ke Xu, Jialin Sun, Shiyue Zhang, Xinyao Jiao, Jie Zhou, Weiwei Shan, Xi Wang, Zhe Jiang, Southeast University, CN Dingrong Pan, National Center of Technology Innovation for Electronic Design Automation, CN; Ning Wang, Nan Guan, City University of Hong Kong, HK; Xinwei Fang, University of York, GB
- **A Post-Implementation Performance Prediction Method with HLS Optimization Directives**
  Jingyu Zhu, Yan Ding, Lu Xiao, Kenli Li, Chubo Liu, Zheng Xiao, Hunan University, CN
- **Contention-Aware Forecasting of Energy Efficiency Through Sequence-Based Models in Modern Heterogeneous Processors**
  Mohammed Bakr Sikal, Jeferson Gonzalez, Heba Khdr, Joerg Henkel, Karlsruhe Institute of Technology, DE
- **AutoPower: Automated Few-Shot Architecture-Level Power Modeling by Power Group Decoupling**
  Qijun Zhang, Yao Lu, Mengming Li, Zhiyao Xie, Hong Kong University of Science and Technology, HK

Session Chair(s): Peipei Zhou, Brown University; Pi-Cheng Hsiu, Academia Sinica

RIGHT ON TIME, BUILT TO LAST: NEW FRONTIERS IN CRITICAL SYSTEM DESIGN

Time: 3:30 PM - 5:30 PM

Topic Area(s): Systems

Session Type: Research Manuscript

Room: 3008, Level 3

Description: As systems grow more complex, ensuring both time-critical performance and fault tolerance becomes essential for reliability and efficiency. This session showcases cutting-edge research tackling fault resilience, real-time processing, and efficient memory utilization. Topics include advanced ECC for CXL memory, statistical fault tolerance in LLM inference, and automated resource configuration for serverless workflows. Additional highlights cover time-aware traffic shaping (Megabits to Kilobits), DAG modeling for autonomous systems, predictive memory failure management, fault injection for GPGPU graph processing, and flexible error detection in real-time multi-core systems. Join us to explore the latest breakthroughs in resilient, real-time system design.

- **MemSeer: Leveraging Memory Failure Distinctions and Multi-Grained Prediction in Ultra-Scale Heterogeneous X86/ARM Clusters**
  Yunfei Gu, Yixuan Liu, Xinyuan Wu, Bo Shao, Chentao Wu, Jieru Zhao, Jie Li, Minyi Guo, Shanghai Jiao Tong University, CN; Shiyi Li, Harbin Institute of Technology, CN; Kunlin Yang, Wengui Zhang, Feilong Lin, Huawei, CN
- **CXL-ECC: an Efficient LRC-Based on-CXL-Memory-eXpander-Controller ECC to Enhance Reliability and Performance of DRAM Error Correction**
  Yixuan Liu, Yunfei Gu, Junhao Dai, Xinyuan Wu, Chentao Wu, Xinfei Guo, Jieru Zhao, Jie Li, Minyi Guo, Shanghai Jiao Tong University, CN
- **Megabits Down to Kilobits: Memory-Efficient Time-Aware Shaping for TSN**
  Xuyan Jiang, Wenwen Fu, Xiangrui Yang, Yingwen Chen, Zhigang Sun, National University of Defense Technology, CN; Wenfei Wu, Peking University, CN
- **AARC: Automated Affinity-Aware Resource Configuration for Serverless Workflows**
  Lingxiao Jin, Zinuo Cai, Zebin Chen, Hongyu Zhao, Ruhui Ma, Shanghai Jiao Tong University, CN
- **FlexStep: Enabling Flexible Error Detection in Multi/Many-core Real-time Systems**
  Tinglue Wang, Yiming Li, Zhenghui Guo, Zhe Jiang, Southeast University, CN; Wei Tang, University of Southeast at NanJing, CN; Jiapeng Guan, Dalian University of Technology, CN; Renshuang Jiang, National University of Defense Technology, CN; Ran Wei, Lancaster University, GB; Jing Li, New Jersey Institute of Technology, US
- **GraphFI: An Efficient Fault Injection Framework for Graph Processing on GPGPUs**
  Nan Jiang, Hengshan Yue, Jingweijia Tan, Mengting Zhou, Xiaonan Wang, Yuchun Wang, Wenda Wei, Jilin Xiaohui Wei, Jilin University, CN; Meikang Qiu, Dakota State University, US
- **Construction of DAG Models for Autonomous Systems**
  Jing Huang, Kuan Jiang, Wei Liang, Hunan University of Science and Technology, CN; Weijie Wang, Wanli Chang, Hunan University, CN
- **ReaLM: Reliable and Efficient Large Language Model Inference with Statistical Algorithm-Based Fault Tolerance**
  Tong Xie, Jiawang Zhao, Zuodong Zhang, Yuan Wang, Runsheng Wang, Ru Huang, Meng Li, Peking University, CN; Zishen Wan, Georgia Institute of Technology, US

Session Chair(s): Antonino Tumeo, Pacific Northwest National Lab

SCALING, LEARNING, AND PARALLELIZING THE FUTURE OF VERIFICATION AND SYNTHESIS

Time: 3:30 PM - 5:30 PM

Topic Area(s): EDA

Session Type: Research Manuscript

Room: 3003, Level 3

Description: This session explores advanced methods in the verification and validation of design, focusing on scalable, parallel, and learning-driven approaches. Papers presented cover innovations such as GPU-accelerated RTL simulation, fuzzing frameworks for network-on-chip verification, and multi-agent guided optimization for logic synthesis. With a focus on simulation, scaling, and parallelization, the research presented pushes the boundaries of modern verification practices, addressing complex challenges and offering more efficient, automated solutions for large-scale designs.

- **InterConFuzz: A Fuzzing-Based Comprehensive NoC Verification Framework**
  Samit Miftah, Kanad Basu, The University of Texas at Dallas, US; Hyunmin Kim, Technology Innovation Institute, AE
- **Multicore Environment State Representation for Agent-Directed Test Generation**
  Bruno Miranda, Luiz Pereira, Marcio Castro, Luiz Santos, Federal University of Santa Catarina, BR
- **GSIM: Accelerating RTL Simulation for Large-Scale Design**
  Lu Chen, Zihao Yu, Ninghui Sun, Yungang Bao, Institute of Computing Technology, Chinese Academy of Sciences, CNN; Dingyi Zhao, Beijing Institute of Open Source Chip, CN

- **Insights From Rights and Wrongs: A Large Language Model for Solving Assertion Failures in RTL Design**
  Jie Zhou, Yuchen Hu, Xinyao Jiao, Zhe Jiang, Southeast University, CN; Youshu Ji, National Center of Technology Innovation for Electronic Design Automation, CN; Ning Wang, Bingkun Yao, Nan Guan, City University of Hong Kong, HK; Xinwei Fang, University of York, GB; Shuai Zhao, Sun Yat-sen University, CN
- **GEM: GPU-Accelerated Emulator-Inspired RTL Simulation**
  Zizheng Guo, Runsheng Wang, Yibo Lin, Peking University, CN; Yanqing Zhang, Haoxing Ren, Nvidia, US
- **Simulation-Based Parallel Sweeping: A New Perspective on Combinational Equivalence Checking**
  Tianji Liu, Evangeline Young, The Chinese University of Hong Kong, HK
- **MAGCS: Multi-Agent Guided Configuration Search for Optimization Fault Detection in Logic Synthesis**
  Peiyu Zou, Xiaochen Li, Shikai Guo, Dalian Maritime University, CN; Weihong Sun, Yuyao Xu, Hi-Think Technology, Corp, CN; He Jiang, Dalian University of Technology, CN
- **Parallel Dynamic Partitioning for Datapath Combinational Equivalence Checking**
  Shuai Zhou, Weikang Zhang, Zite Jiang, Haihang You, Institute of Computing Technology, Chinese Academy of Sciences, CN; Xindi Zhang, Shaowei Cai, Institute of Software, Chinese Academy of Sciences, CN

Session Chair(s): Chung-Yang Huang, National Taiwan University; Nan Wu, George Washington University

SKIP THE BITS!: INNOVATIVE ARITHMETIC, ARCHITECTURE, CO-DESIGN FOR AI

Time: 3:30 PM - 5:30 PM

Topic Area(s): AI

Session Type: Research Manuscript

Room: 3000, Level 3

Description: In this session, we explore innovative strategies that combine alternate arithmetic approaches, novel architectures, and co-design techniques to enhance AI systems. Focusing on both theoretical and practical advancements, the session highlights how new arithmetic methods and specialized hardware, including sparsity handling and approximation, are driving improvements in performance and efficiency for AI models. More specifically, the session presents various microarchitectures for efficient processing such as bit-sparse attention architecture, bit-level sparse MAC architecture, and dense-sparse systolic array architecture, and novel arithmetic such as Polar form and floating-point approximation. It also includes emerging accelerator architectures including Gaussian Splatting and Point-Cloud Processing.

- **Blaze: An Efficient Bit-Sparse Attention Architecture with Workload Orchestration Optimization**
  Runzhou Zhang, Faxian Sun, Yiming Wang, Kunchen Zou, Zhinan Qin, Jianli Chen, Jun Yu, Kun Wang, Fudan University, CN
- **DenSparSA: A Balanced Systolic Array Approach for Dense and Sparse Matrix Multiplication**
  Ziheng Wang, Ruiqi Sun, An Zou, Shanghai Jiao Tong University, CN; Xin He, University of Michigan, US; Tianrui Ma, Institute of Computing Technology, Chinese Academy of Sciences, CN
- **UniCoS: A Unified Neural and Accelerator Co-Search Framework for CNNs and ViTs**
  Wei Fu, Wenqi Lou, Cheng Tang, Hongbing Wen, Yunji Qin, Lei Gong, Chao Wang, Xuehai Zhou, University of Science and Technology of China, CN
- **GSAcc: Accelerate 3D Gaussian Splatting via Depth Speculation and Gaussian-Centric Rasterization**
  Mengtian Yang, Yipeng Wang, Chieh-Pu Lo, Xiuhao Zhang, Sirish Oruganti, Jaydeep Kulkarni, The University of Texas at Austin, US
- **High-Throughput Point-Cloud Accelerator with Sparsity-Aware Hierarchical Neighbor Voxel Search and Skipping**
  Yun Chia Yu, Suraj Putlur Narasimha Reddy, Aryan Devrani, Anirudh Srinivasan,; Saianudeep Reddy Nayini, Sohyeon Kim, Mingu Kang, University of California, San Diego, US; Sung-Joon Jang, Sang-Seol Lee, Korea Electronics Technology Institute (KETI), KR
- **April: Accuracy-Improved Floating-Point Approximation For Neural Network Accelerators**
  Yonghao Chen, Xinyu Chen, The Hong Kong University of Science and Technology, CN; Jiaxiang Zou, University of Electronic Science and Technology of China, CN
- **CVMAX: Accelerator Architecture with Polar Form Multiplication for Complex-Valued Neural Networks**
  Hyunwuk Lee, Sungbin Kim, Sungwoo Kim, Won Woo Ro, Yonsei University, KR
- **An Efficient Bit-Level Sparse MAC-Accelerated Architecture with SW/HW Co-Design on FPGA**
  Chenming Zhang, Lei Gong, Chao Wang, Xuehai Zhou, University of Science and Technology of China, CN

Session Chair(s): Debjyoti Bhattacharjee, IMEC; Minah Lee, Georgia Institute of Technology

THE RISE OF AI, GPUS & PROCESSORS: THE NEXT-GEN ARCHITECTURES

Time: 3:30 PM - 5:30 PM

Topic Area(s): Design

Session Type: Research Manuscript

Room: 3002, Level 3

Description: This session highlights cutting-edge research on advancing next-gen computing architectures, focusing on processors, GPUs, and AI-enhanced systems. Papers explore incremental partitioning techniques on GPUs, fine-grain instruction analysis in out-of-order superscalar processors, and multi-core solutions with AI extensions for multimodal LLMs. Additional topics include efficient hardware resource sharing in GPU sub-cores, a multi-fidelity optimization framework for microarchitecture design space exploration (e.g., RISCV), new GPU kernel fusion techniques, and dataflow optimizations for tensor accelerators. These works showcase innovative strategies that push the boundaries of performance, scalability, and efficiency in modern computing systems.

- **IG-Kway: Incremental K-Way Graph Partitioning on GPU**
  Wan Luan Lee, Dian-Lun Lin, Che Chang, Boyang Zhang, Yi-Hua Chung, Tsung-Wei Huang, University of Wisconsi, Madison, US; Shui Jiang, Tsung-Yi Ho, The Chinese University of Hong Kong, HK; Ulf Schlichtmann, Technical University of Munich, DE
- **FireGuard: A Generalized Microarchitecture for Fine-Grained Security Analysis on OoO Superscalar Cores**
  Zhe Jiang, Southeast University, CN; Sam Ainsworth, University of Edinburgh, GB; Timothy Jones, University of Cambridge, GB
- **EdgeMM: Multi-Core CPU with Heterogeneous AI-Extension and Activation-Aware Weight Pruning for Multimodal LLMs at Edge**
  Kangbo Bai, Le Ye, Ru Huang, Tianyu Jia, Peking University, CN
- **ACRS: Adjacent Computation Resource Sharing among Partitioned GPU Sub-Cores**
  Penghao Song, Chongxi Wang, Chenji Han, Jian Wang, Institute of Computing Technology, China Academy of Sciences, CN; Haoyu Zhao, Tingting Zhang, Loongson Technology Co. Ltd, CN; Tianyi Liu, University of Texas at San Antonio, US
- **Swift or Exact? Boosting Efficient Microarchitecture DSE via Multi-fidelity Partial Order Prediction**
  Hang Liu, Gongshang University, CN; Hao Geng, ShanghaiTech University, CN; Zhuolun He, The Chinese University of Hong Kong, HK; Qi Sun, Cheng Zhuo, Zhejiang University, CN
- **Principle-Based Dataflow Optimization for Communication Lower Bound in Operator-Fused Tensor Accelerator**
  Lei Xu, Chen Yin, Zelong Yuan,; Weiguang Sheng, Jianfei Jiang, Qin Wang, Naifeng Jing, Shanghai Jiao Tong University, CN
- **GoPTX: Fine-Grained GPU Kernel Fusion by PTX-level Instruction Flow Weaving**
  Kan Wu, Zejia Lin, Mengyue Xi, Zhongchun Zheng, Wenxuan Pan, Xianwei Zhang, Yutong Lu, Sun Yat-sen University, CN
- **DARIS: An Oversubscribed Spatio-Temporal Scheduler for Real-Time DNN Inference on GPUs**
  Amir Fakhim Babaei, Thidapat (Tam) Chantem, Virginia Tech, US

Session Chair(s): Guy Eichler, Columbia University

ADDITIONAL MEETINGS

HACK at DAC

Sunday, June 22

8:00 AM - 6:00 PM

Monday, June 23

8:00 AM - 6:00 PM

Level 2 Lobby

Young Fellows Kick-Off and All-Day Activities

Sunday, June 22

9:00 AM - 6:00 PM

Room 3018

DAC Early Career Workshop

Sunday, June 22

9:00 AM - 6:00 PM

Room 3006

ICLAD GenAI Chip Hackathon

Sunday, June 22

9:00 AM - 6:00 PM

Room 3012

Sunday Special SKYTalk

Sunday, June 22

5:00 PM - 6:00 PM

Room 3002

Annual Board Meeting of the ACM TODAES

Monday, June 23

11:00 AM - 12:00 PM

Room 3018

ACM SIGDA Business Meeting (Open to Public)

Monday, June 23

2:00 PM - 4:00 PM

Room 3018

IEEE CEDA Distinguished Panel Luncheon

Tuesday, June 24

12:00 PM - 1:30 PM

Room 3016/3018

Birds of a Feather

Tuesday, June 24

6:30 PM - 9:30 PM

Room 3001

Young Fellows Posters

Tuesday, June 24

4:00 PM - 6:00 PM

Level 2 Lobby

PhD Forum & University Demo

Tuesday, June 24

7:00 PM - 9:00 PM

Level 2 Lobby

HACK at DAC & On-Device Generative AI for Science Awards

Tuesday, June 24

3:30 PM - 5:30 PM

Room 3012

Young Fellows Closing Ceremony

Wednesday, June 25

3:30 PM - 5:00 PM

Room 3012

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